Pisces:

A Scalable and Efficient Persistent Transactional Memory

Jinyu Gu, Qianqian Yu, Xiayang Wang, Zhaoguo Wang,
Binyu Zang, Haibing Guan, Haibo Chen

IPADS
INSTITUTE OF PARALLEL
AND DISTRIBUTED SYSTEMS

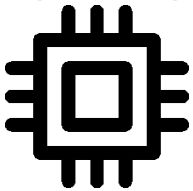
上海交通大學
SHANGHAI JIAO TONG UNIVERSITY

NVM Revolution

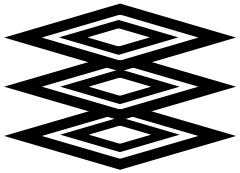
- Non-volatile memory (NVM) is revolutionizing memory and storage

Phase-change memory (PCM)

Resistive Random-access Memory (ReRAM)



Intel/Micron 3D-XPoint



Industrialization: Intel 3D-Xpoint

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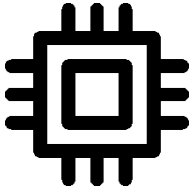

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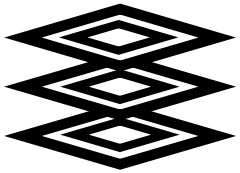
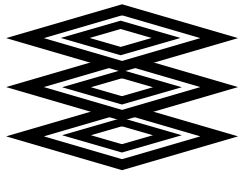


- The recent release of Intel Optane DC Persistent Memory (3D-XPoint) marks the transition of NVM technology from research prototypes to mainstream products

NVM Features

Intel/Micron 3D-XPoint



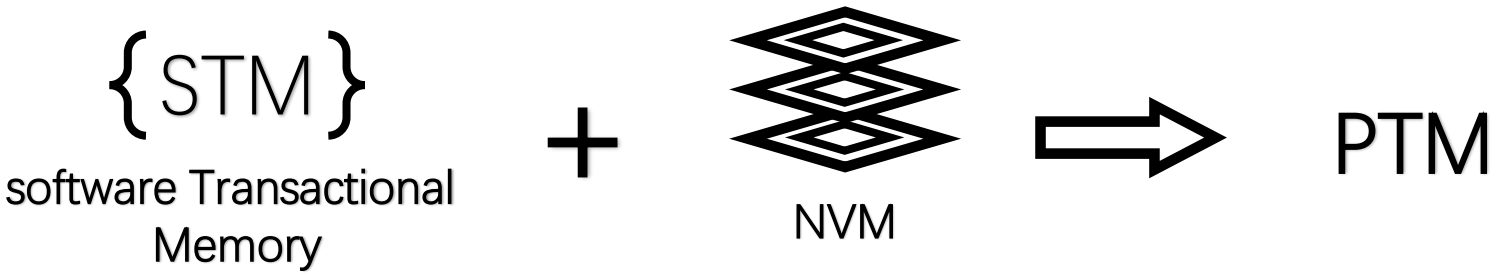
- Byte-addressability
- Non-volatility (high speed)
- Low read latency and high persistency cost

10x write latency comparing with DRAM

Programming Abstraction for NVM

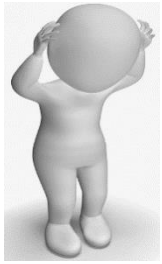
- Persistent Transactional Memory (PTM)
  - *transaction* is a widely-used abstraction
  - an efficient abstraction for programming on persistent memory:

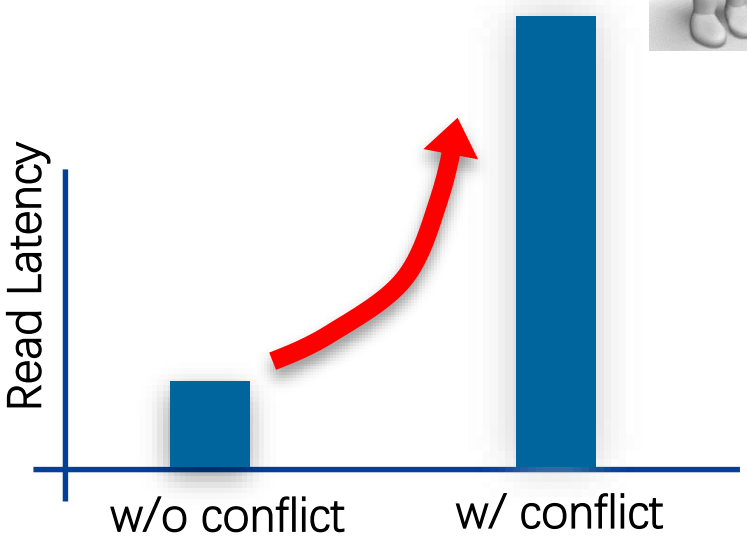
    i.e., builds *transactional memory* abstraction over *NVM*



Existing PTM Issues

read-deficiency





Cause: exposing high NVM persistence overhead to readers

Existing PTM Issues

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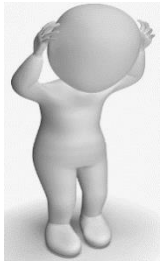
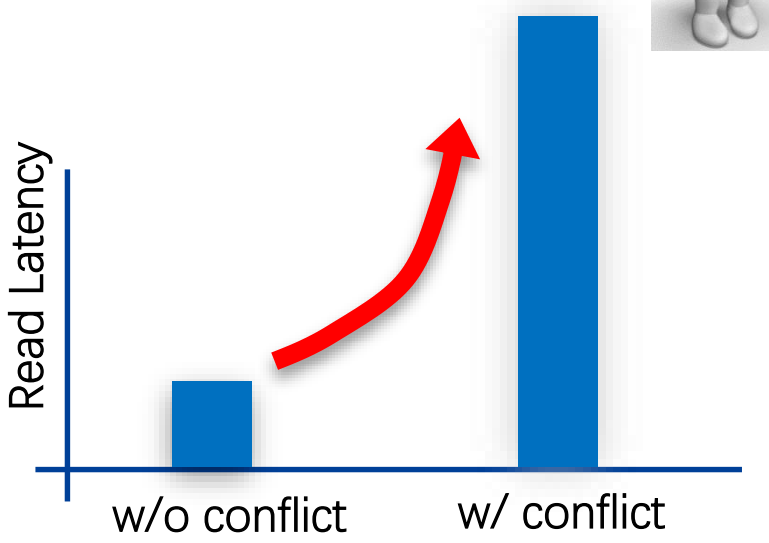
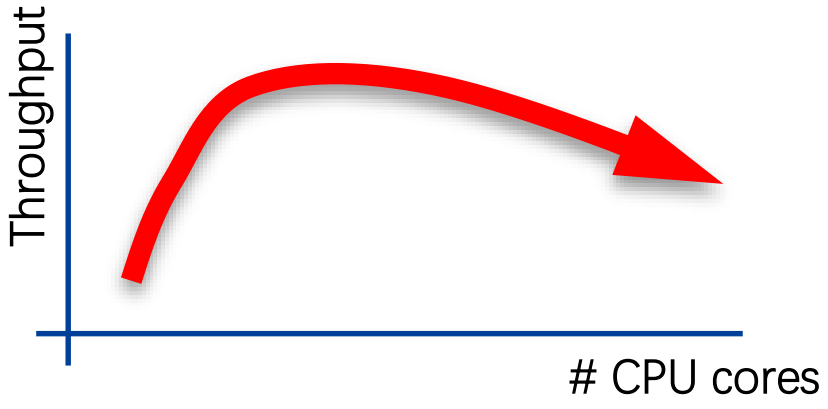




Cause: exposing high NVM persistence overhead to readers

low-scalability



Cause: over-constraining NVM persistence ordering

read-deficiency

low-scalability

Can a PTM achieve both read-efficiency and high-scalability?

Cause: exposing high NVM persistence overhead to readers

Cause: over-constraining NVM persistence ordering

Reuse redo logs as new versions

Dual-version con-currency control

Three-stage commit

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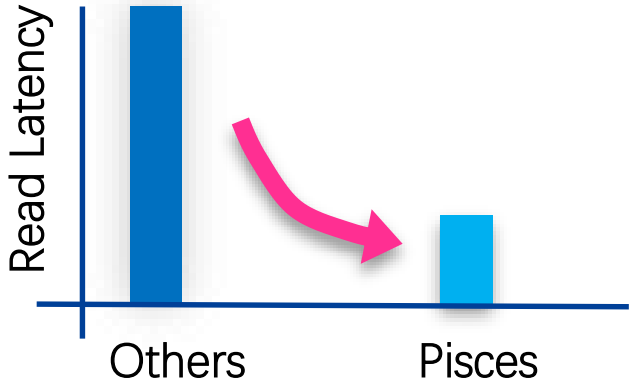
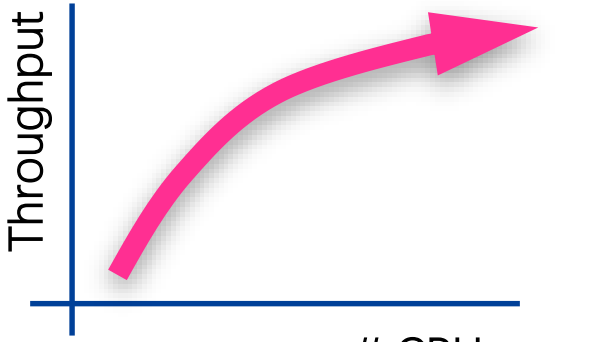
read-efficiency



high-scalability



Thanks & Welcome

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ATC 2019, 11:25 am, Track I, on July 12th

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