

Practical Erase Suspension for Modern Low-latency SSDs

Shine Kim^{†§} Jonghyun Bae[†] Hakbeom Jang^{*} Wenjing Jin[†] Jeonghun Gong[†]
Seoungyeon Lee[§] Tae Jun Ham[†] Jae W. Lee[†]



[†]Seoul National University

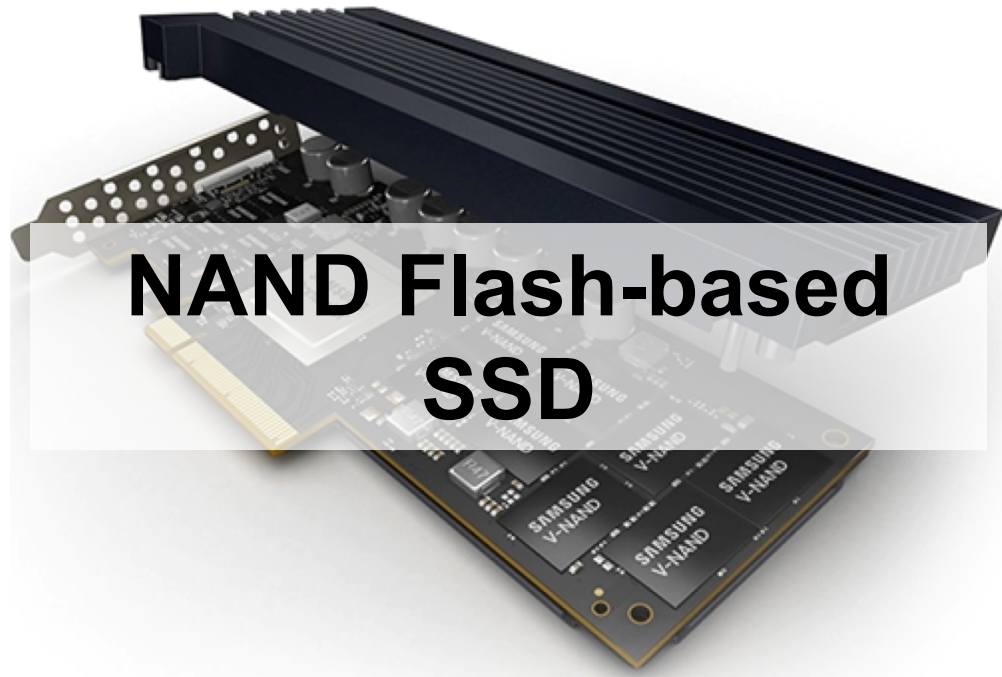
SAMSUNG

[§]SAMSUNG Electronics

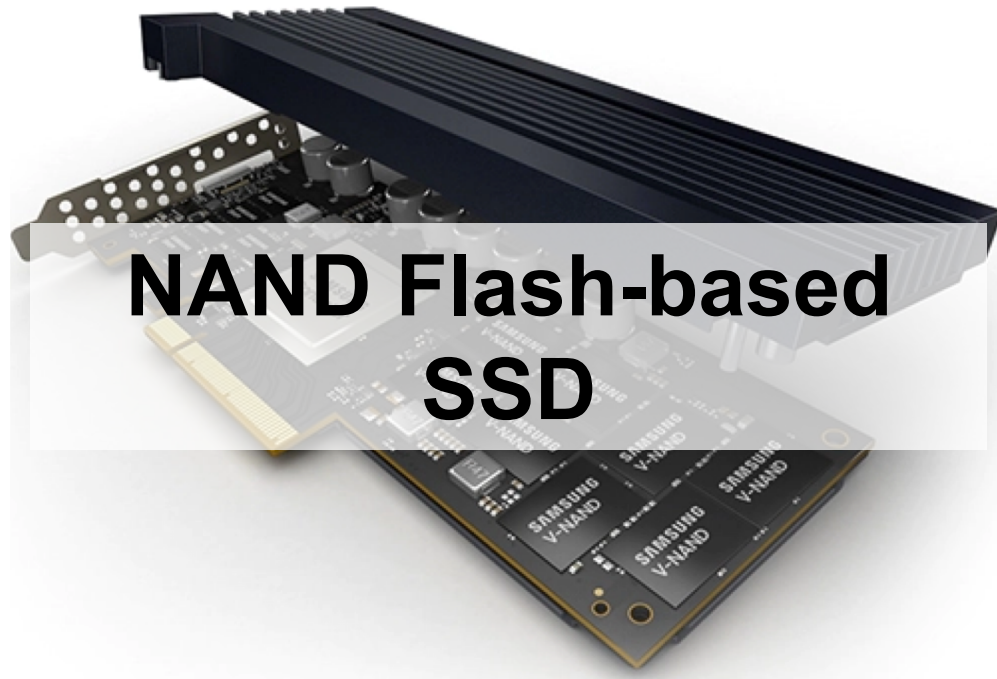


^{*}Sungkyunkwan University

NAND Flash-based SSD



NAND Flash-based SSD

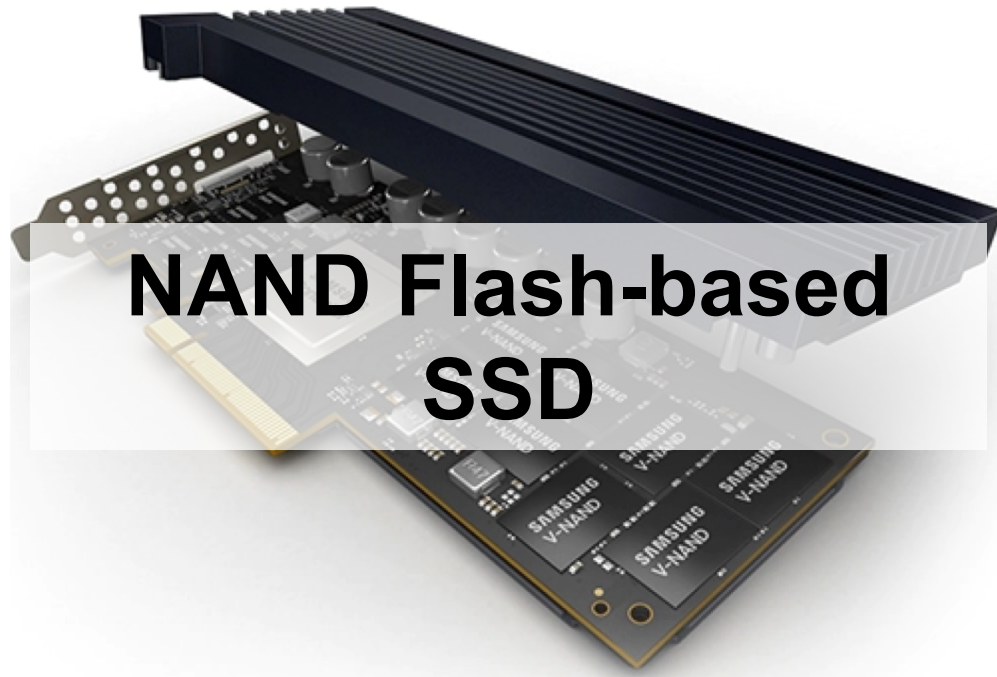


1) Superior Throughput
(e.g., Sequential Read → 6.4GB/s)

2) Low average Latency
(e.g., 4KB Random Read QD1 → 15us)

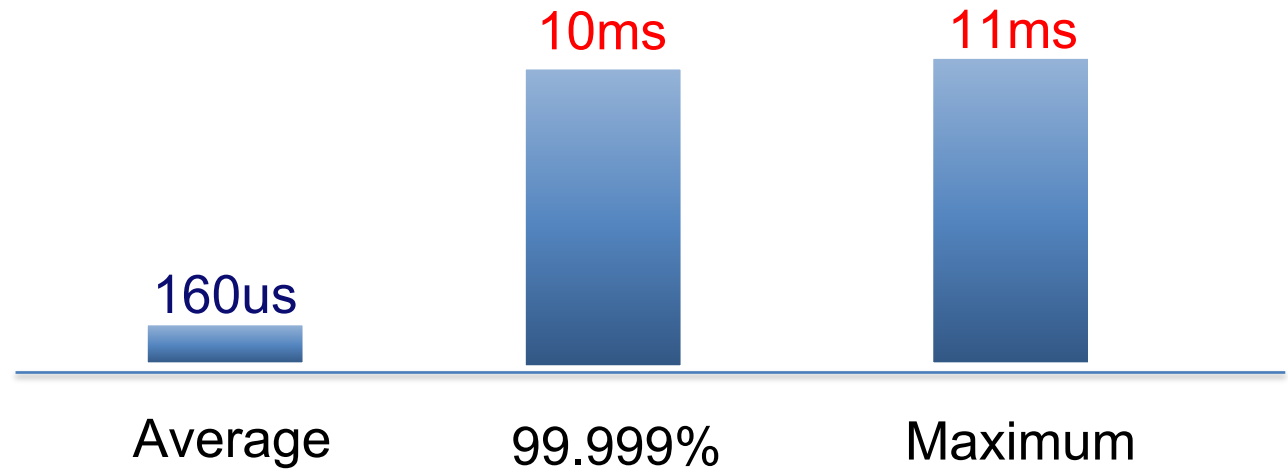
3) Relatively Low Price
(e.g., QLC SSD → 0.1\$/GB)

NAND Flash-based SSD



Read Latency

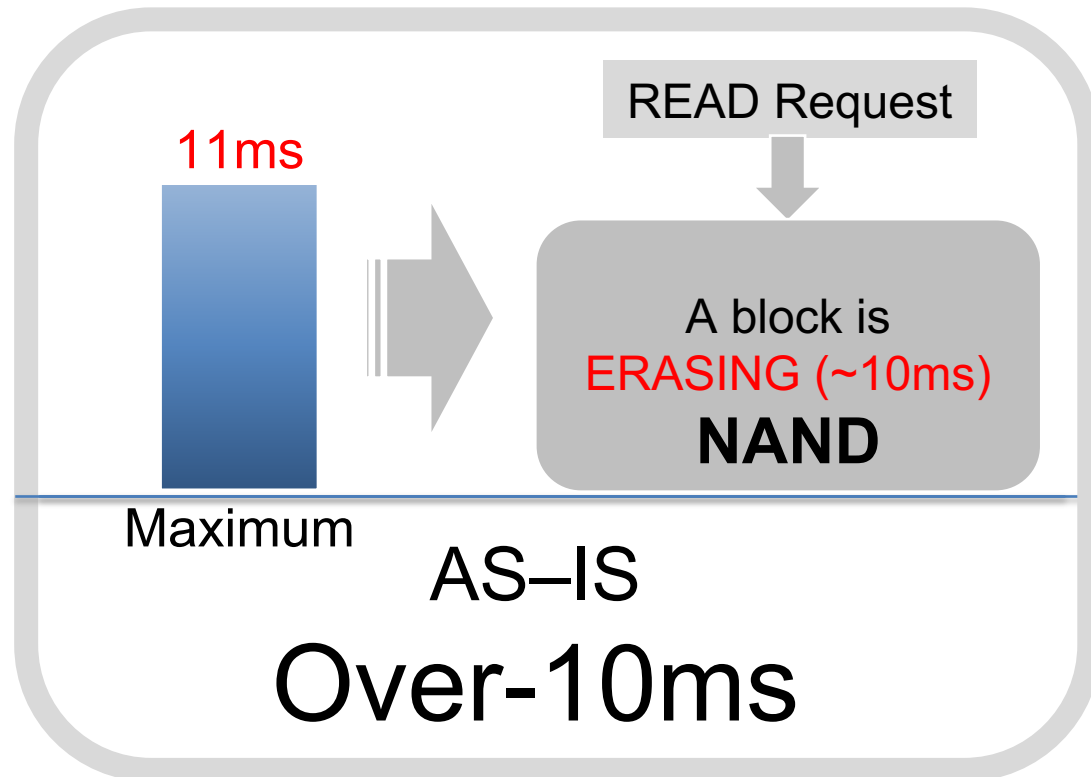
(4KB Random, Read 70%, Write 30%, QD 16)



The source of long read tail latency

Read Tail Latency

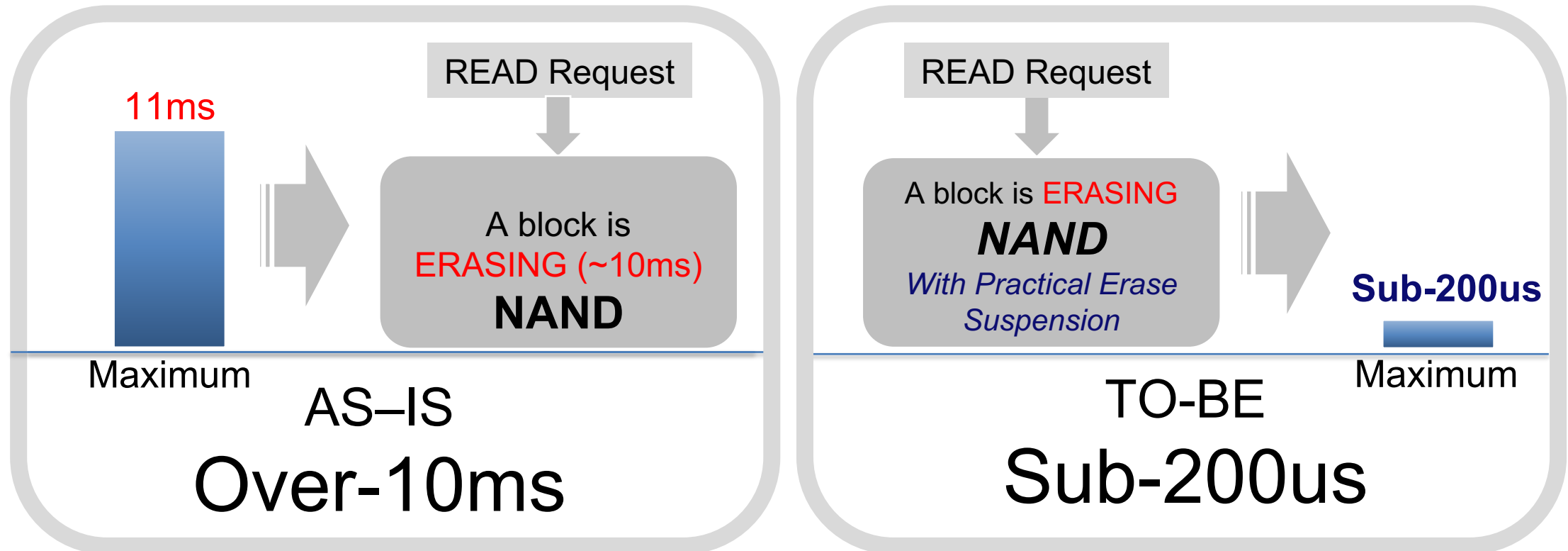
(4KB Random, Read 70%, Write 30%, QD 16)



The source of long read tail latency

Read Tail Latency

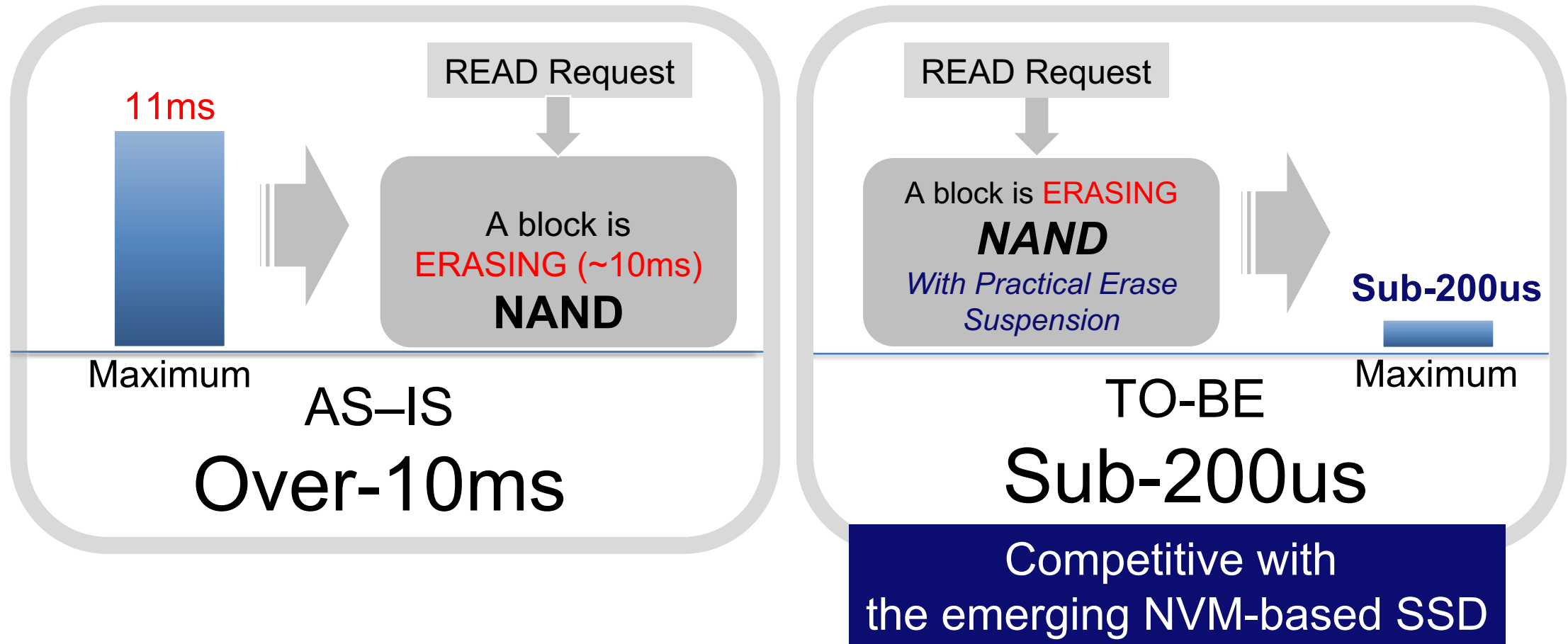
(4KB Random, Read 70%, Write 30%, QD 16)



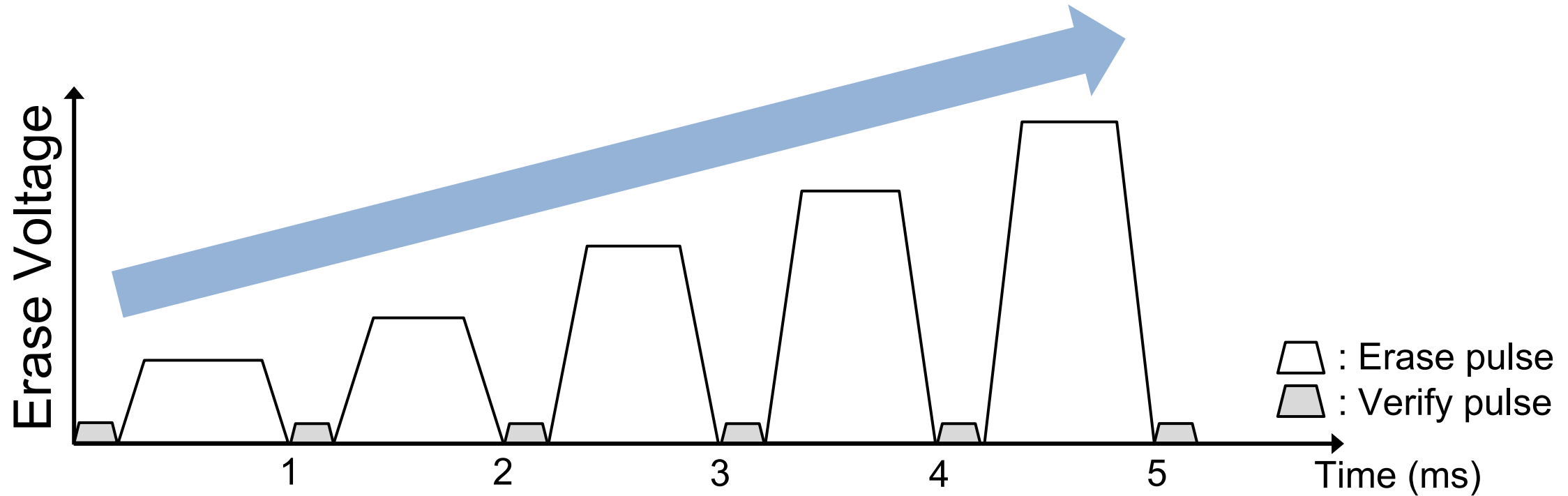
The source of long read tail latency

Read Tail Latency

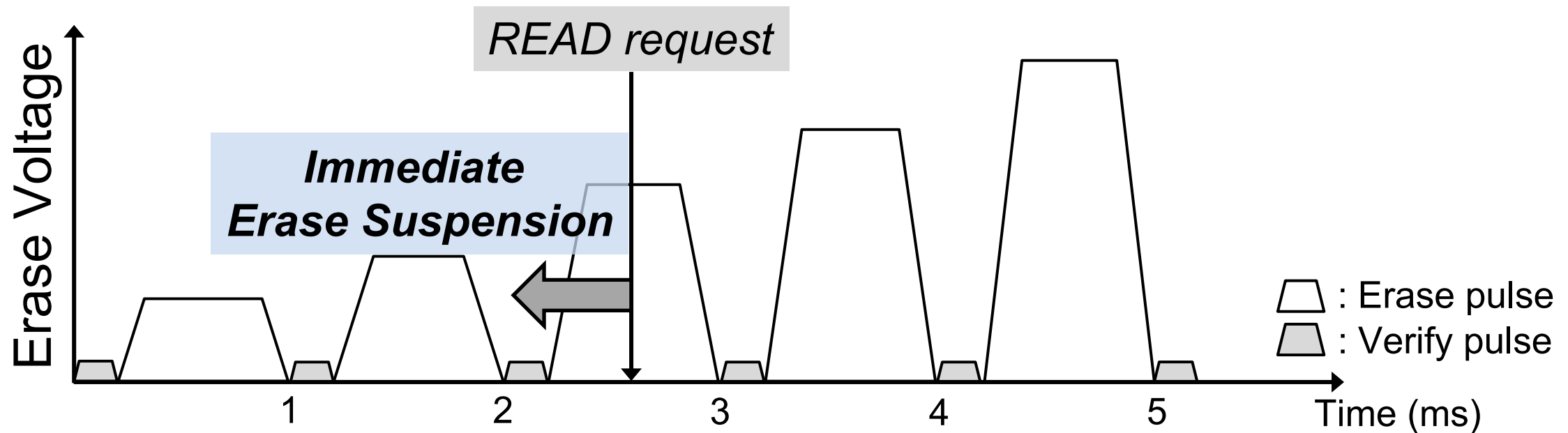
(4KB Random, Read 70%, Write 30%, QD 16)



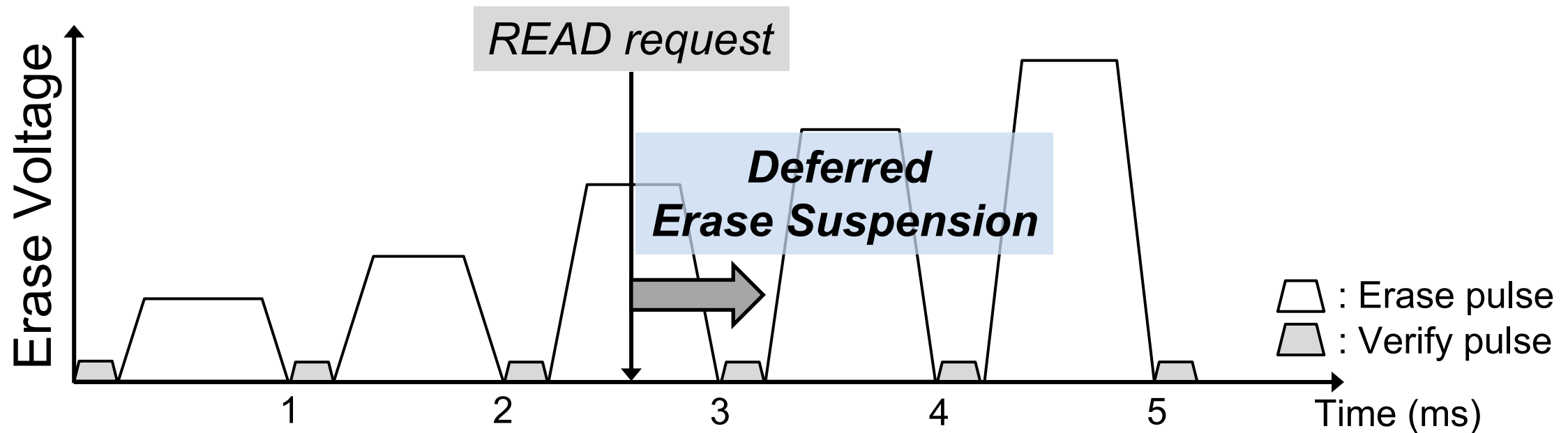
Incremental Step Pulse Erasing (ISPE) scheme



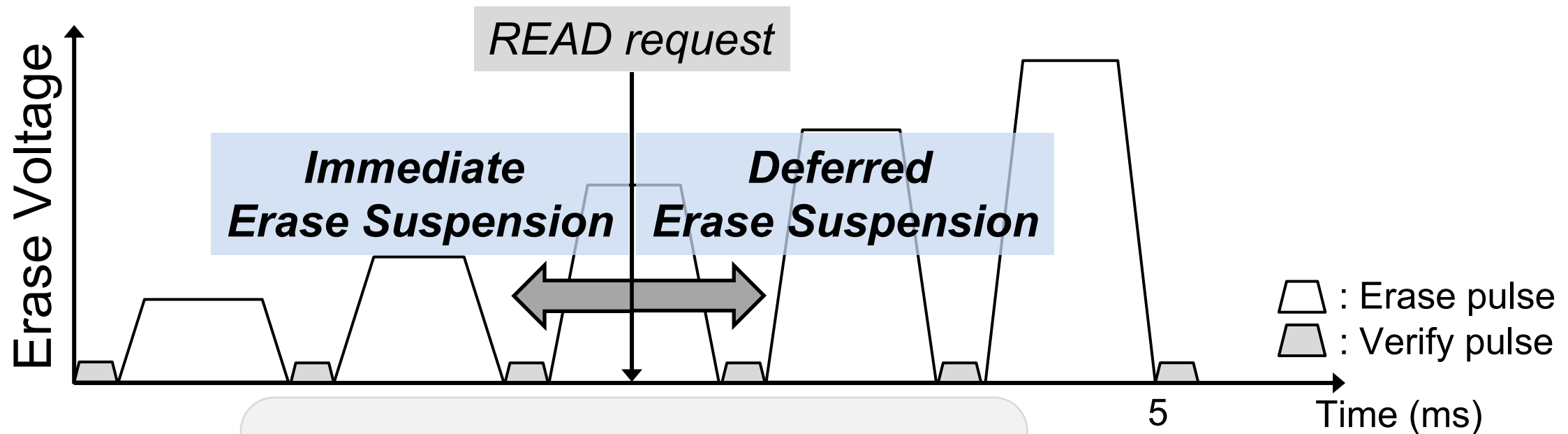
Suspending/Resuming at well-aligned safe points



Suspending/Resuming at well-aligned safe points



Suspending/Resuming at well-aligned safe points



**Timeout-based
switching mechanism**

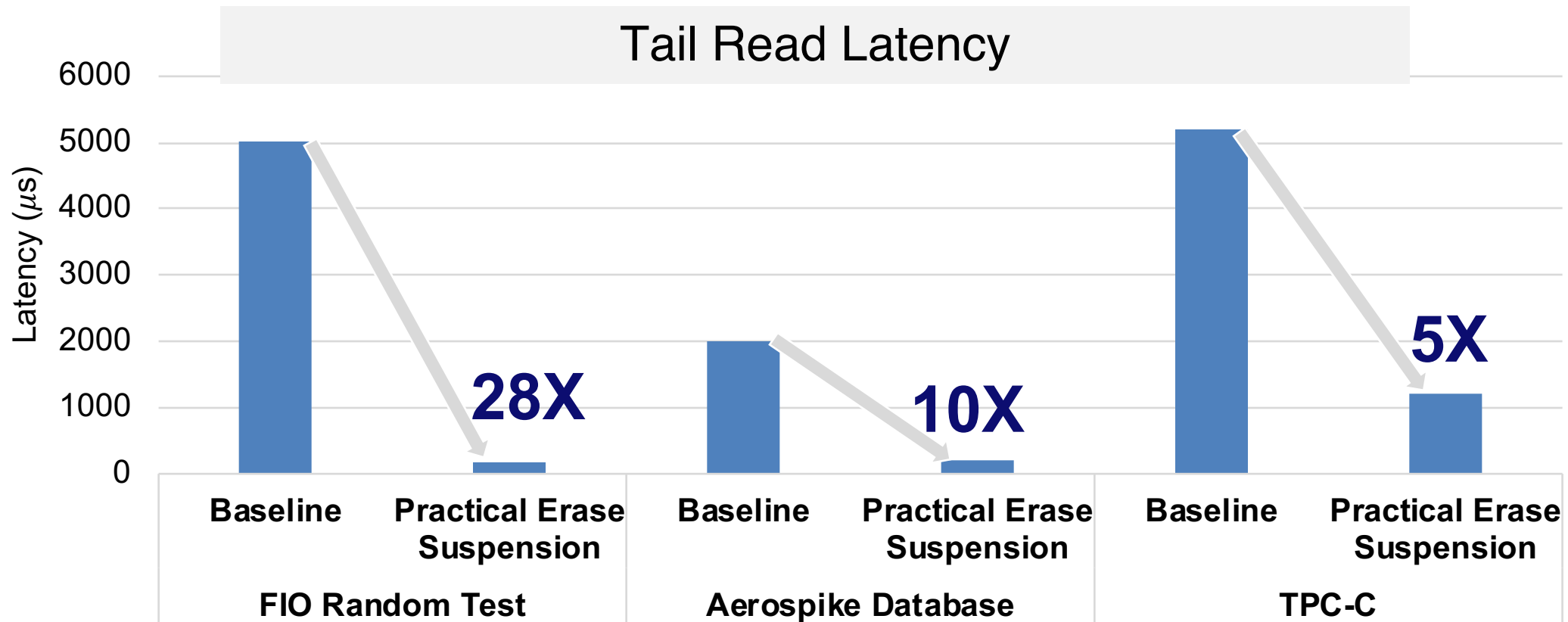
Summary

- **Practical erase suspension harnesses the full potential of NAND flash-based SSDs**



Summary

- **Practical erase suspension harnesses the full potential of NAND flash-based SSDs**



Thank You 😊

USENIX ATC'19

Track I

Solid-State & Hard Disk Drives Session

July 12th 09:55am