# A Double-Edged Sword: **Security Threats and Opportunities** in One-Sided Network Communication

Shin-Yeh Tsai Yiying Zhang

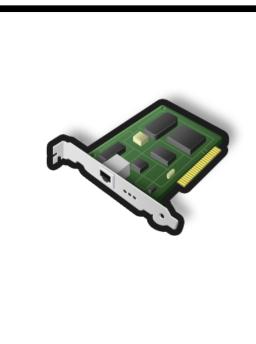


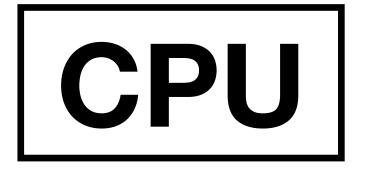












Memory



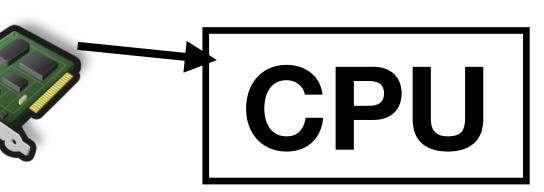


**GET Key-50** 





# **Traditional (Two-sided communication)**



Memory



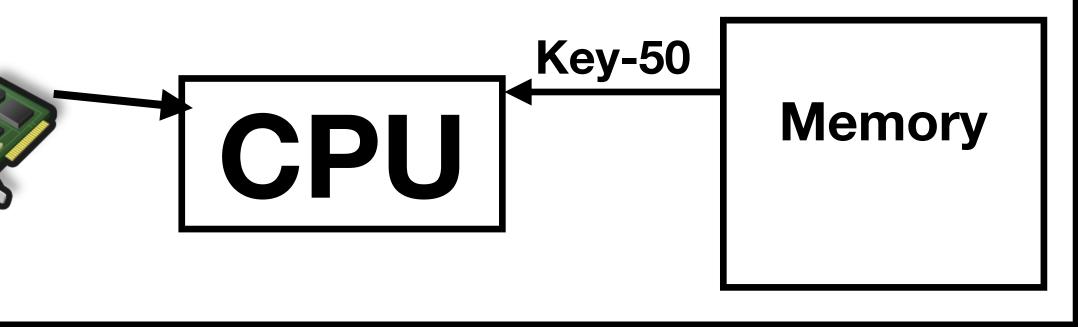


**GET Key-50** 



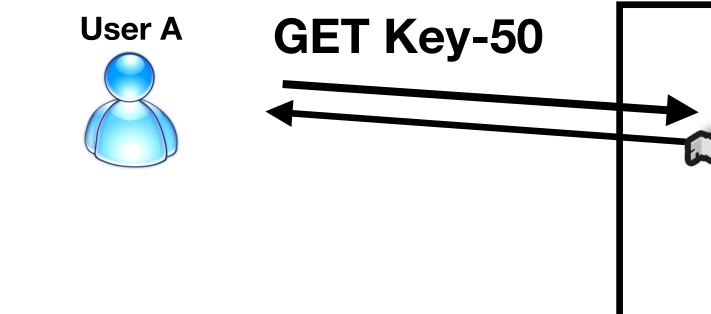


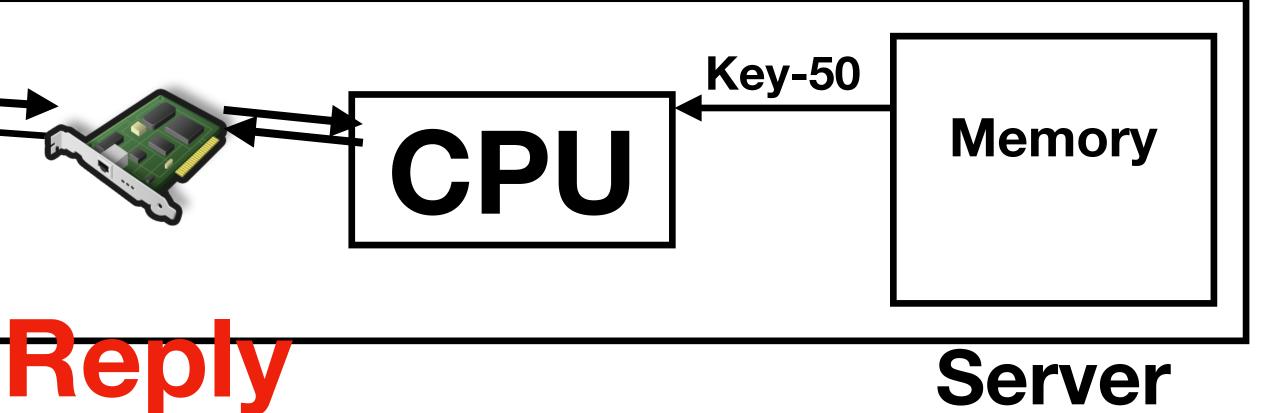
## **Traditional (Two-sided communication)**



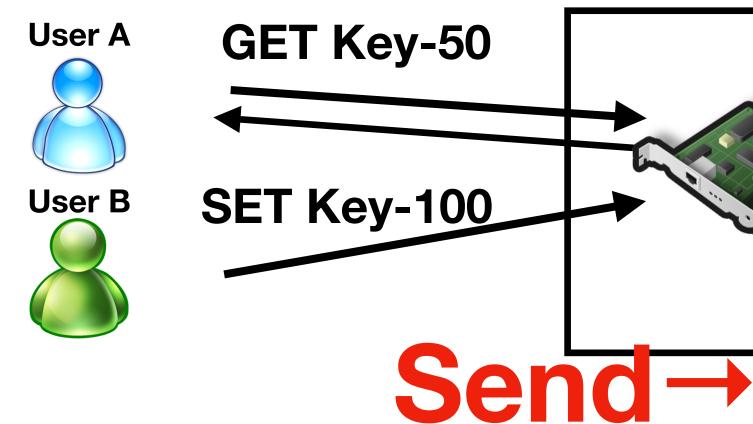


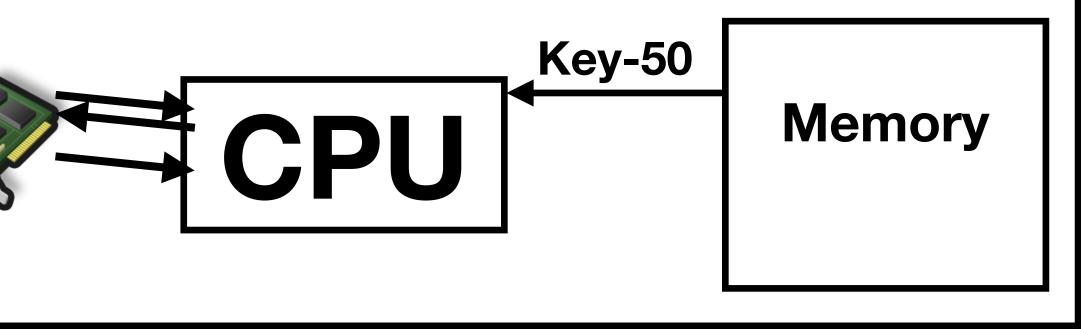




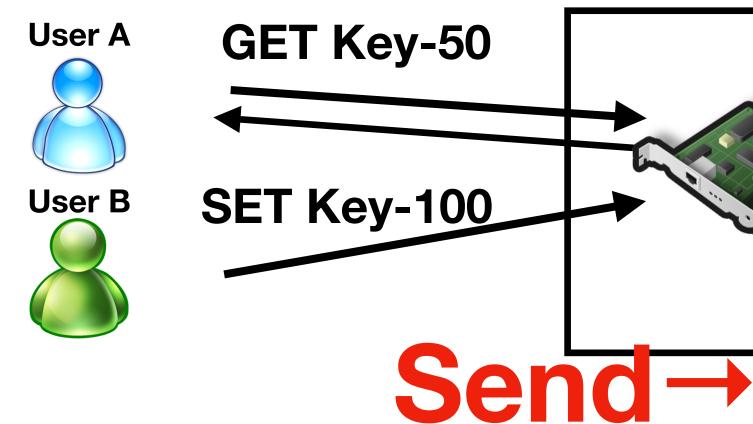


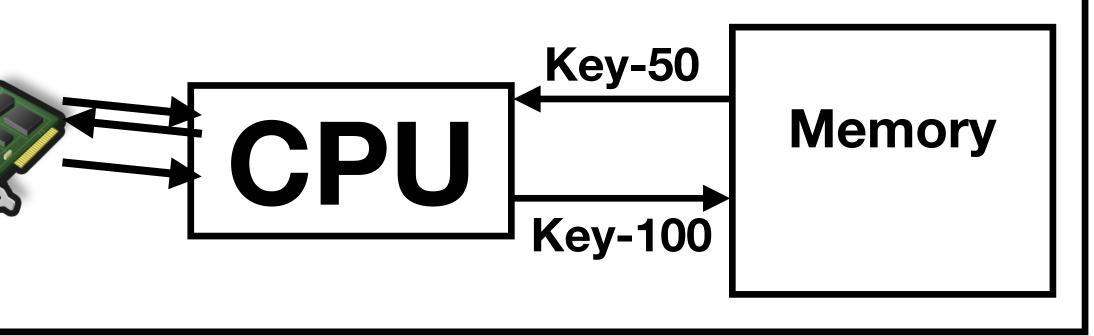




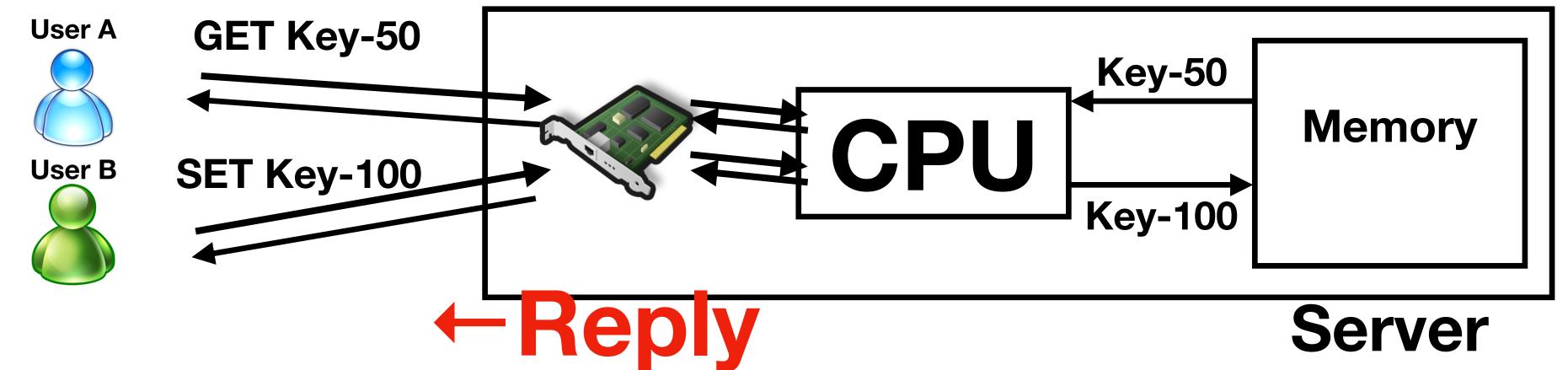




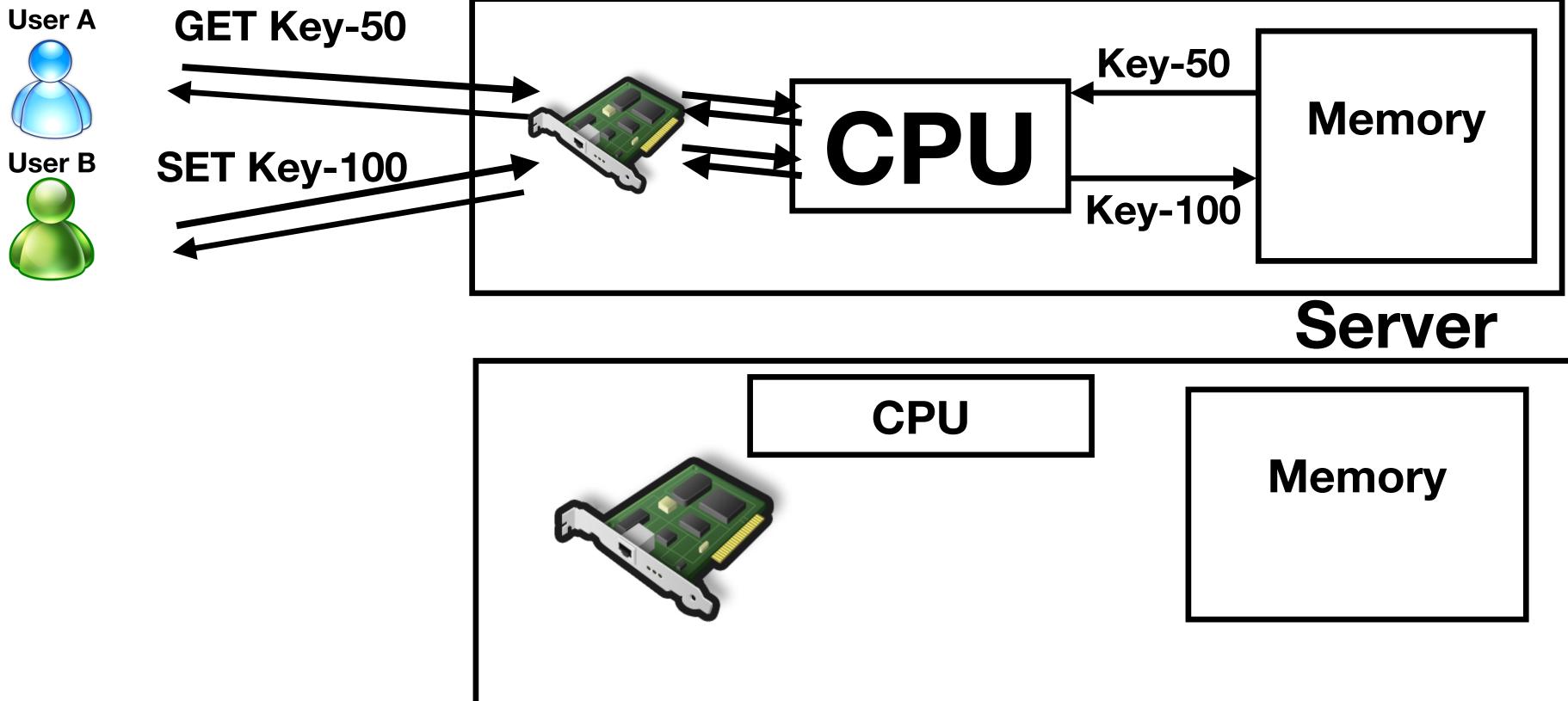


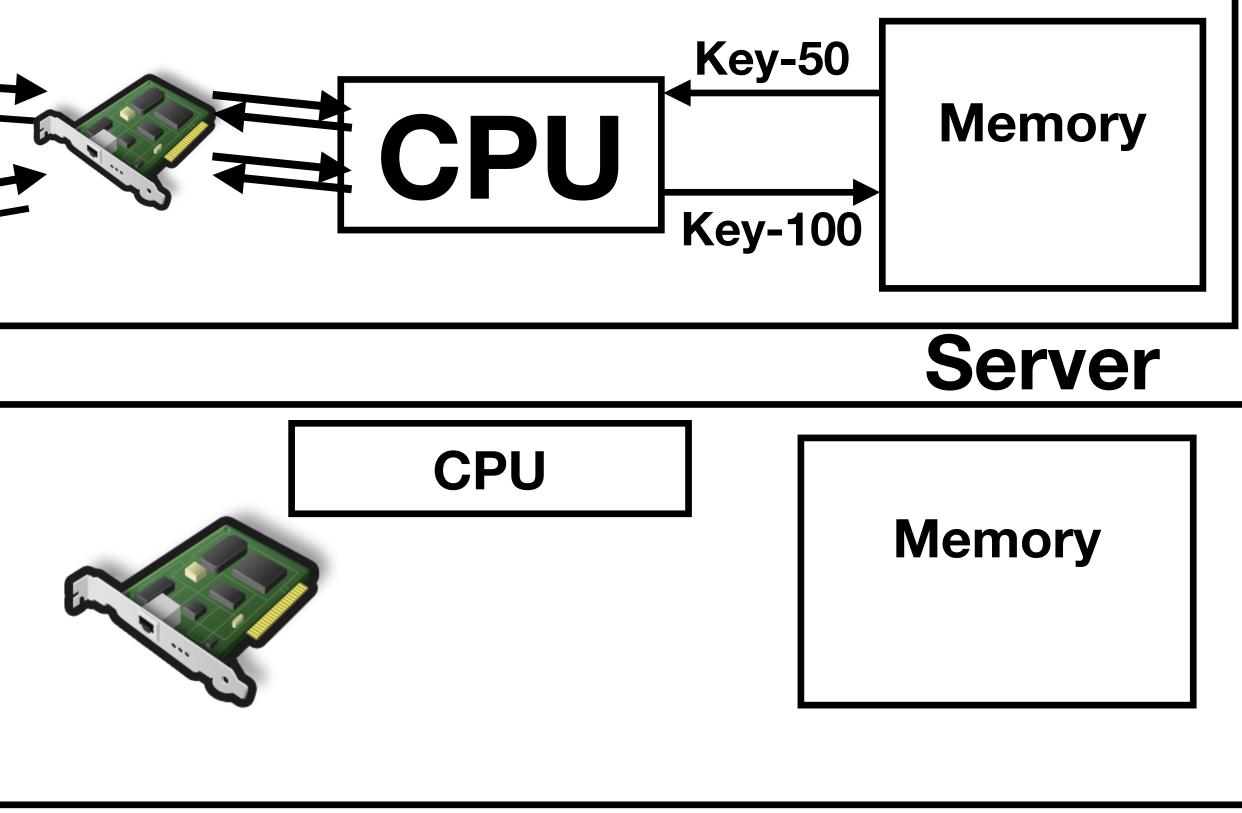




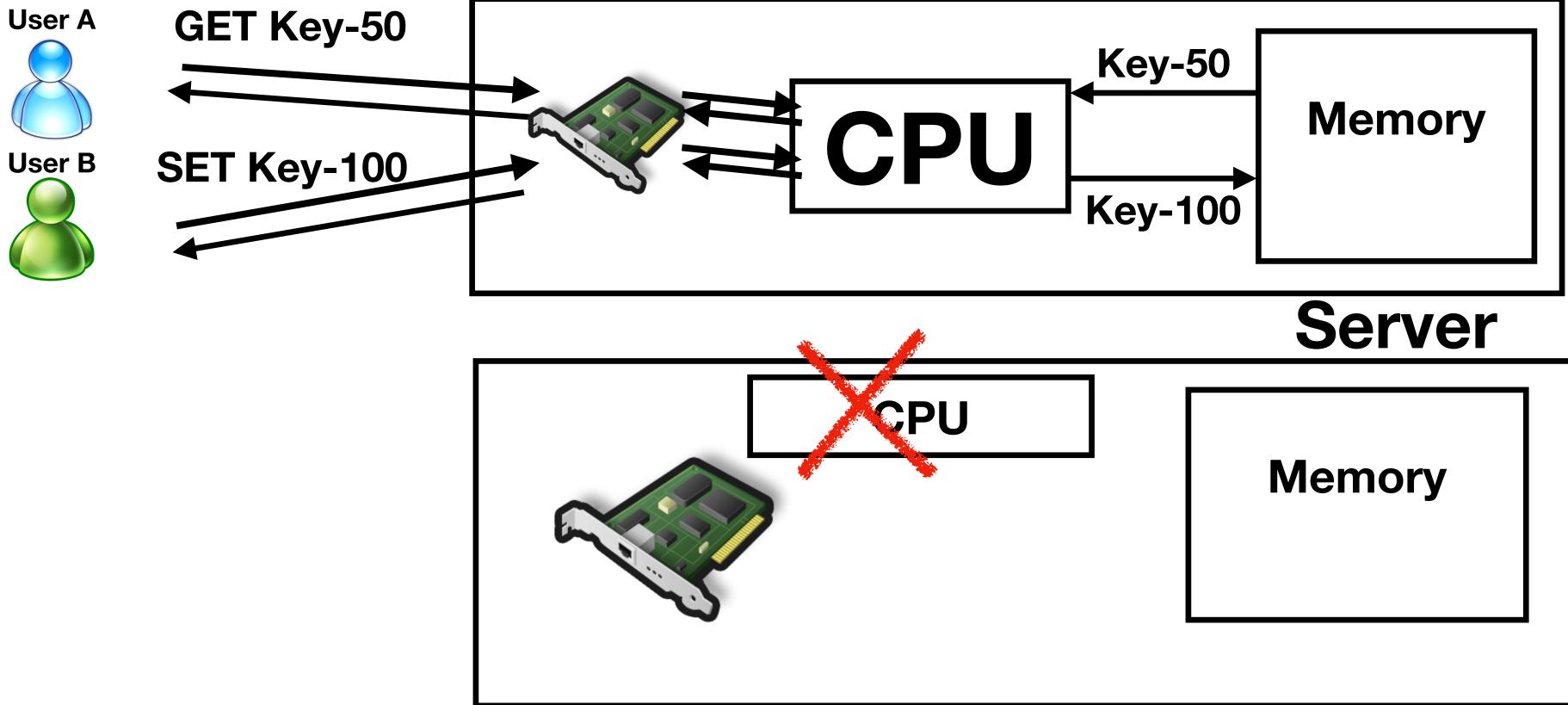


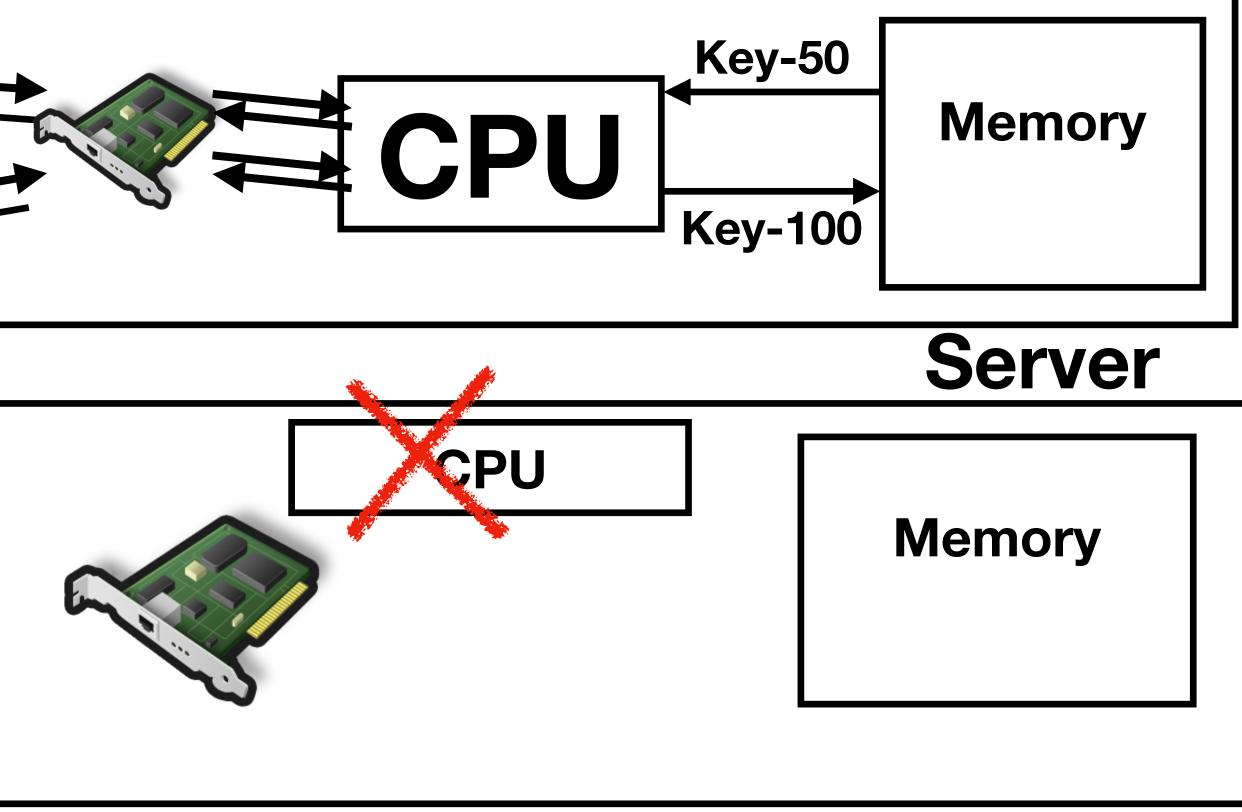




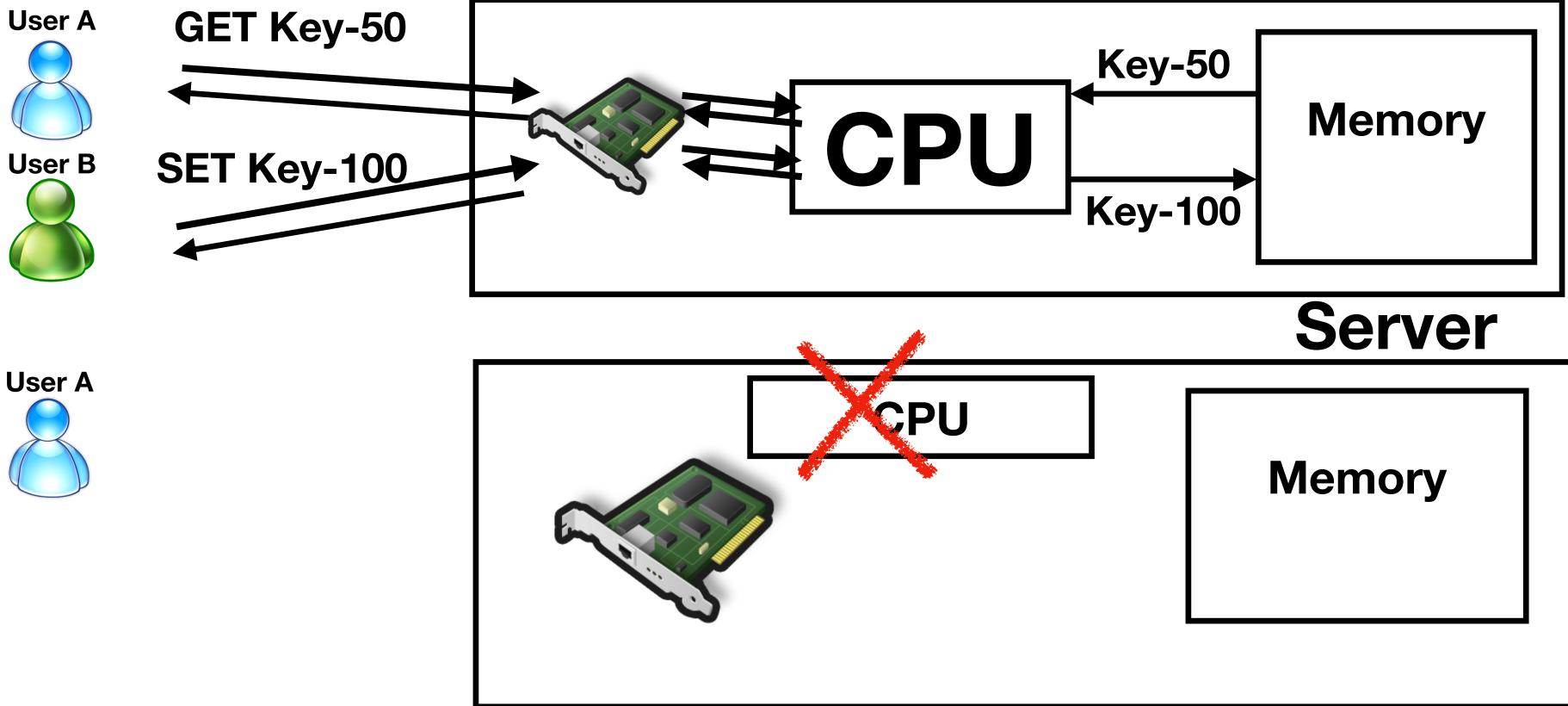




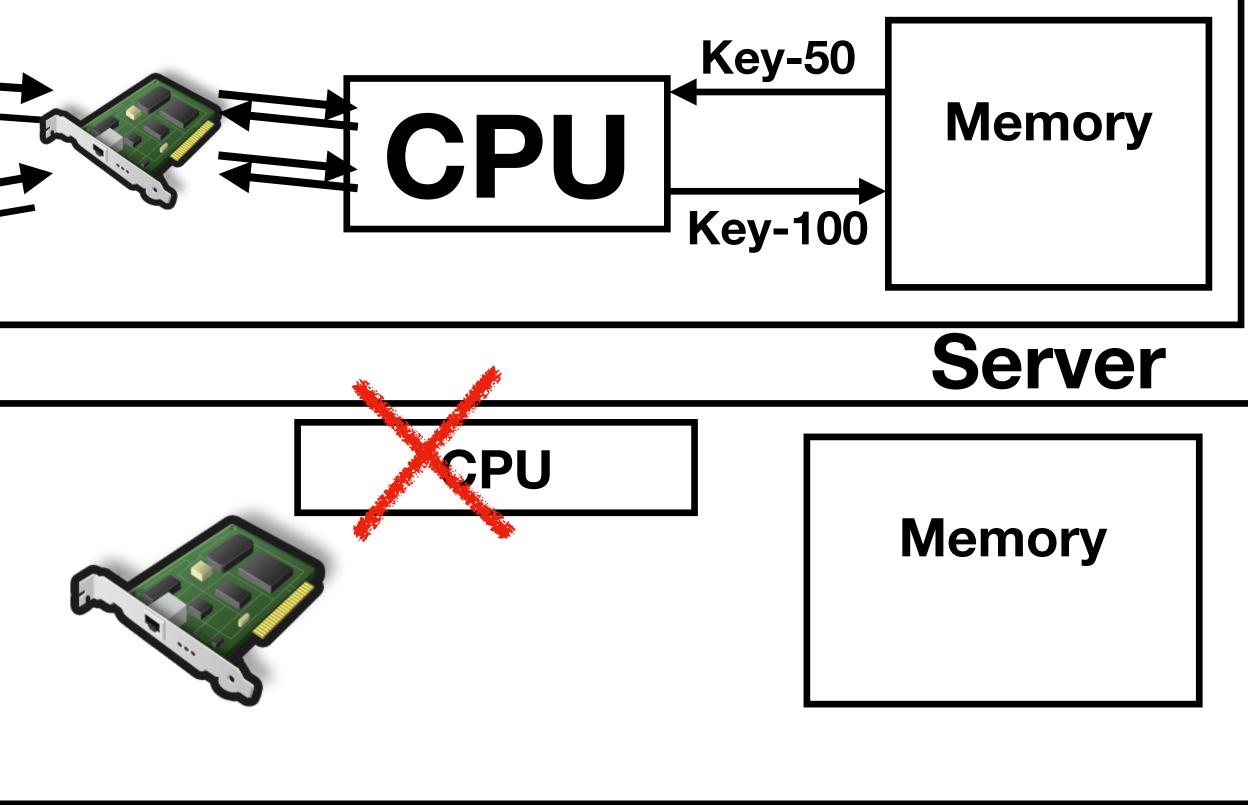




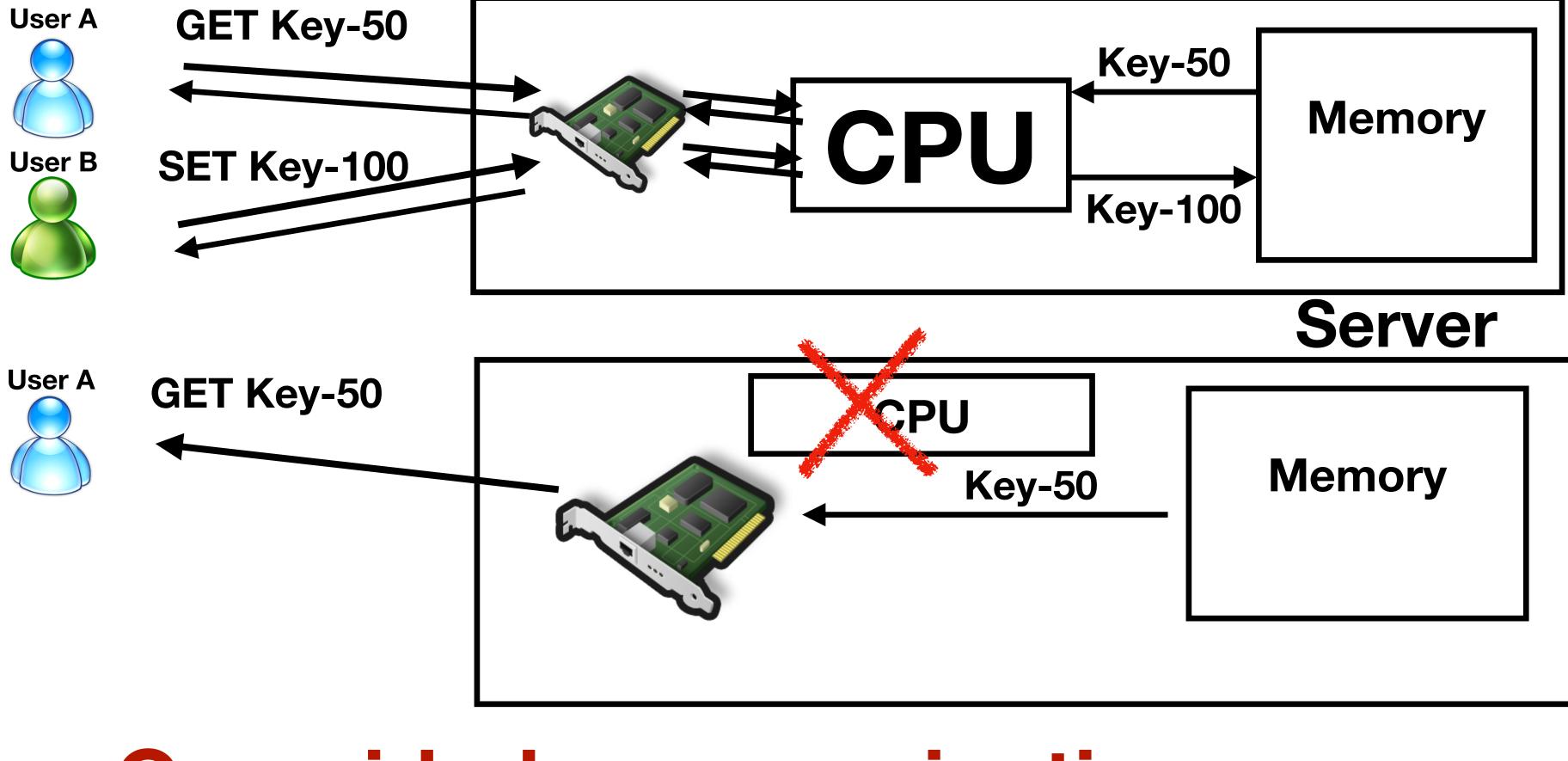




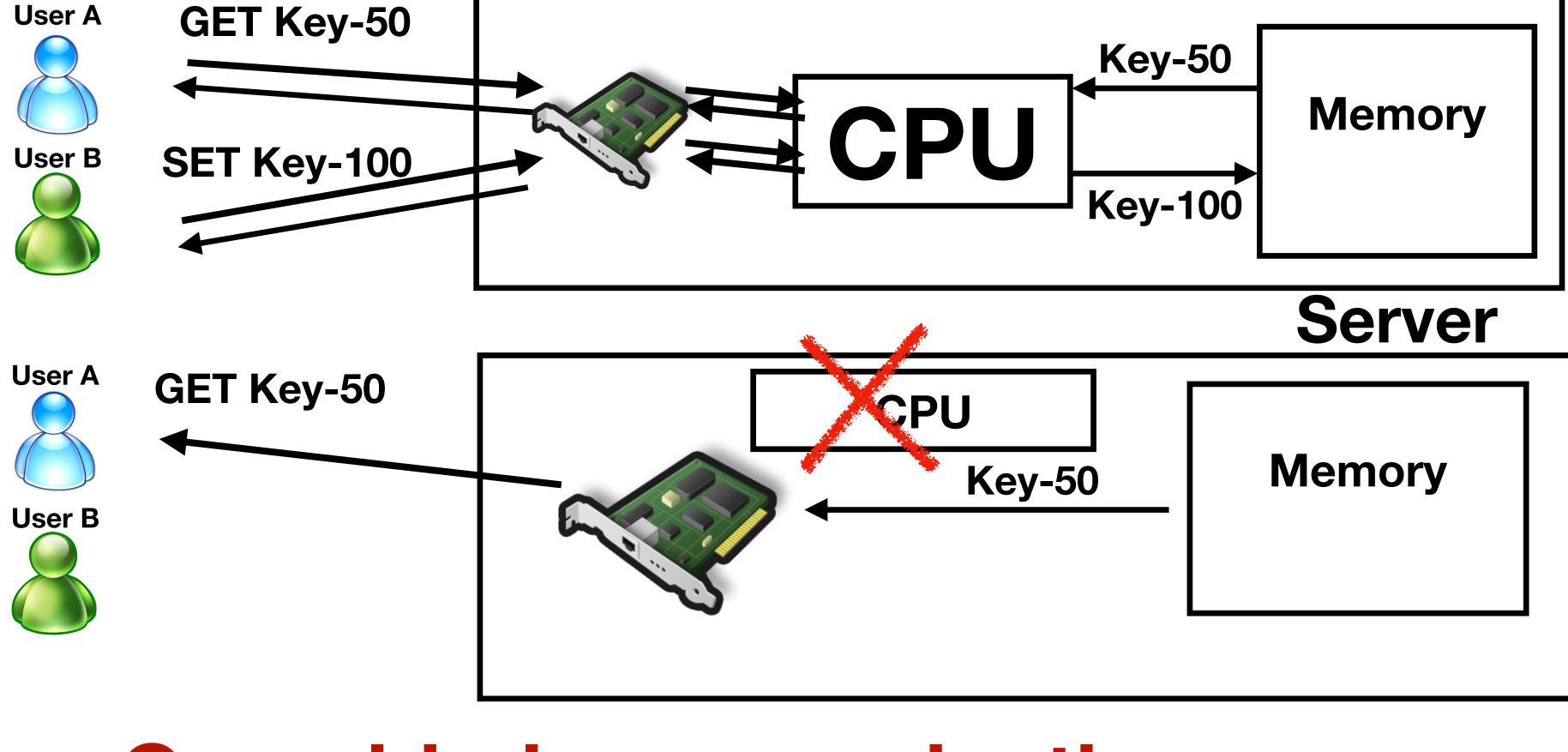




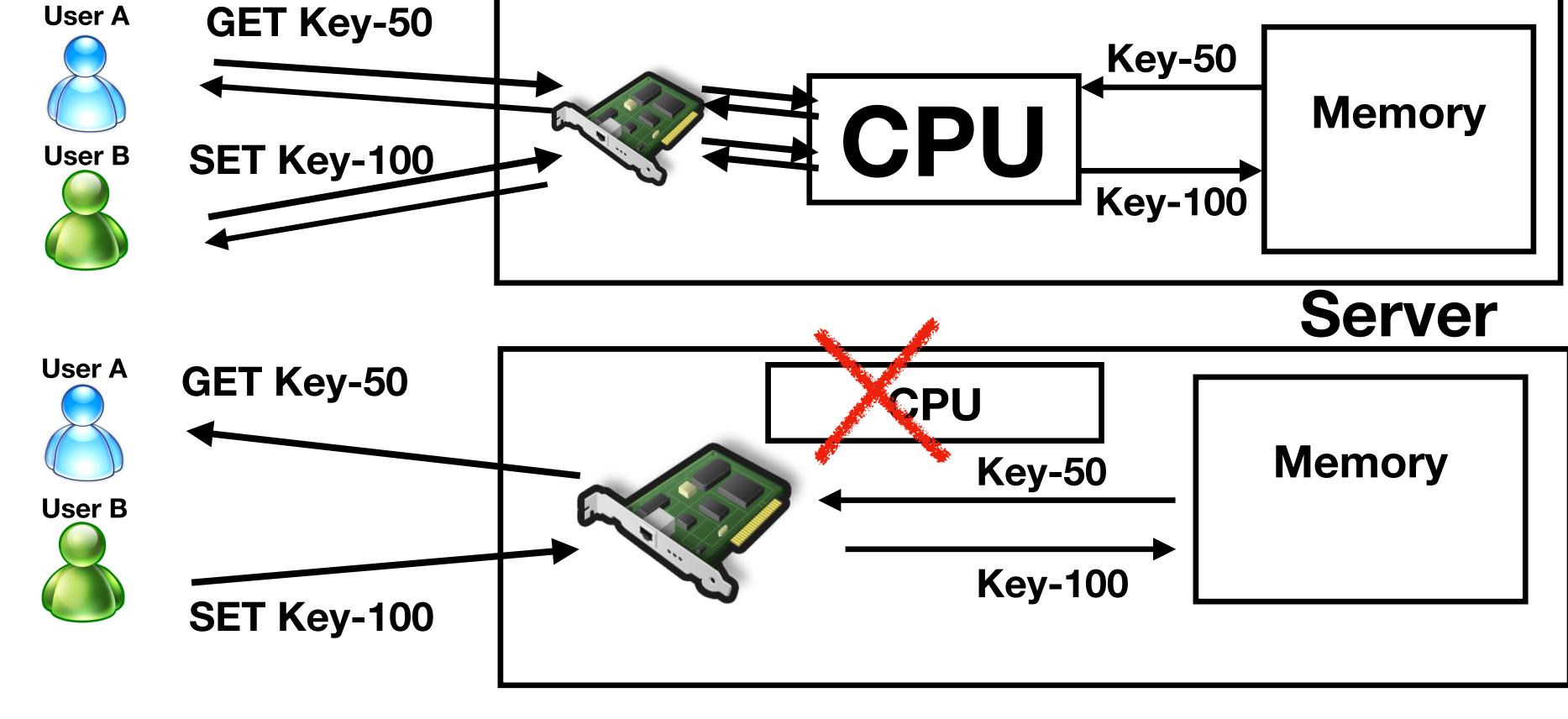














## RDMA

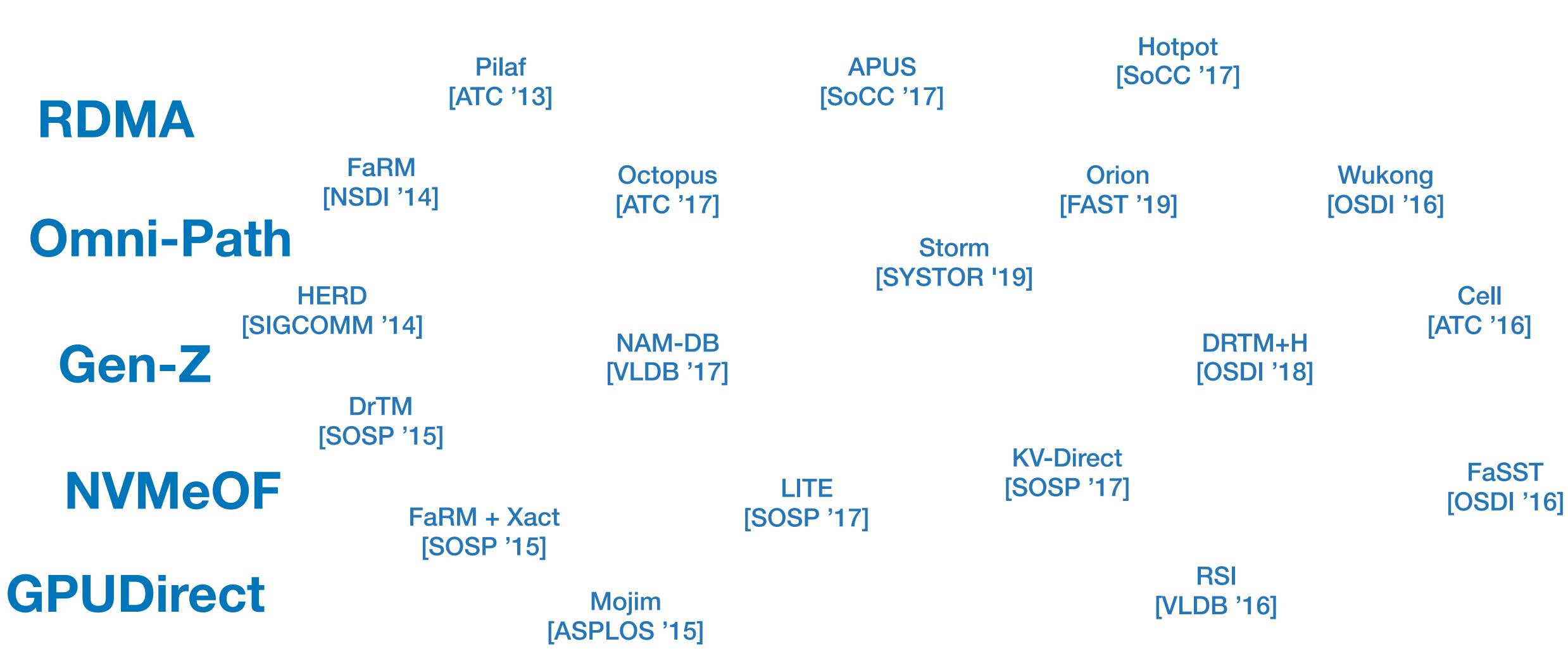
## **Omni-Path**

## Gen-Z

## NVMeOF

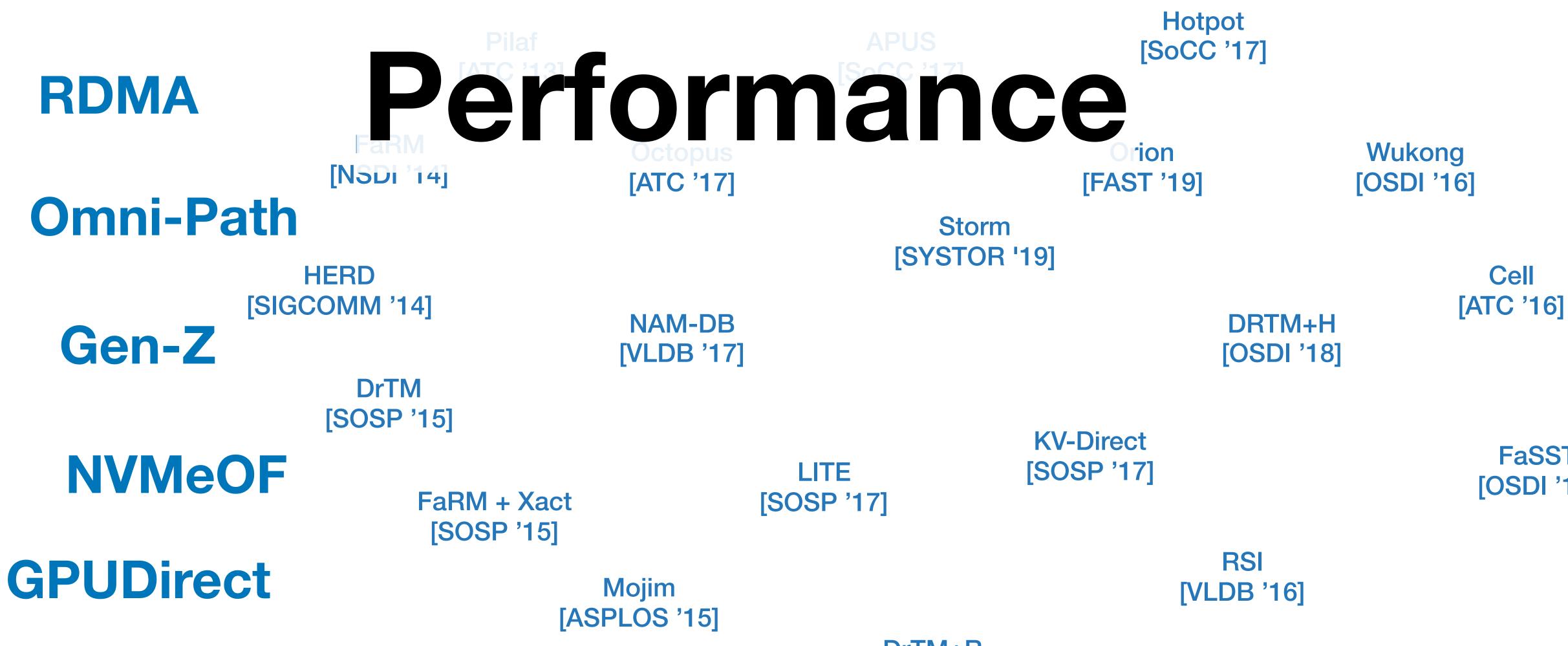
## GPUDirect









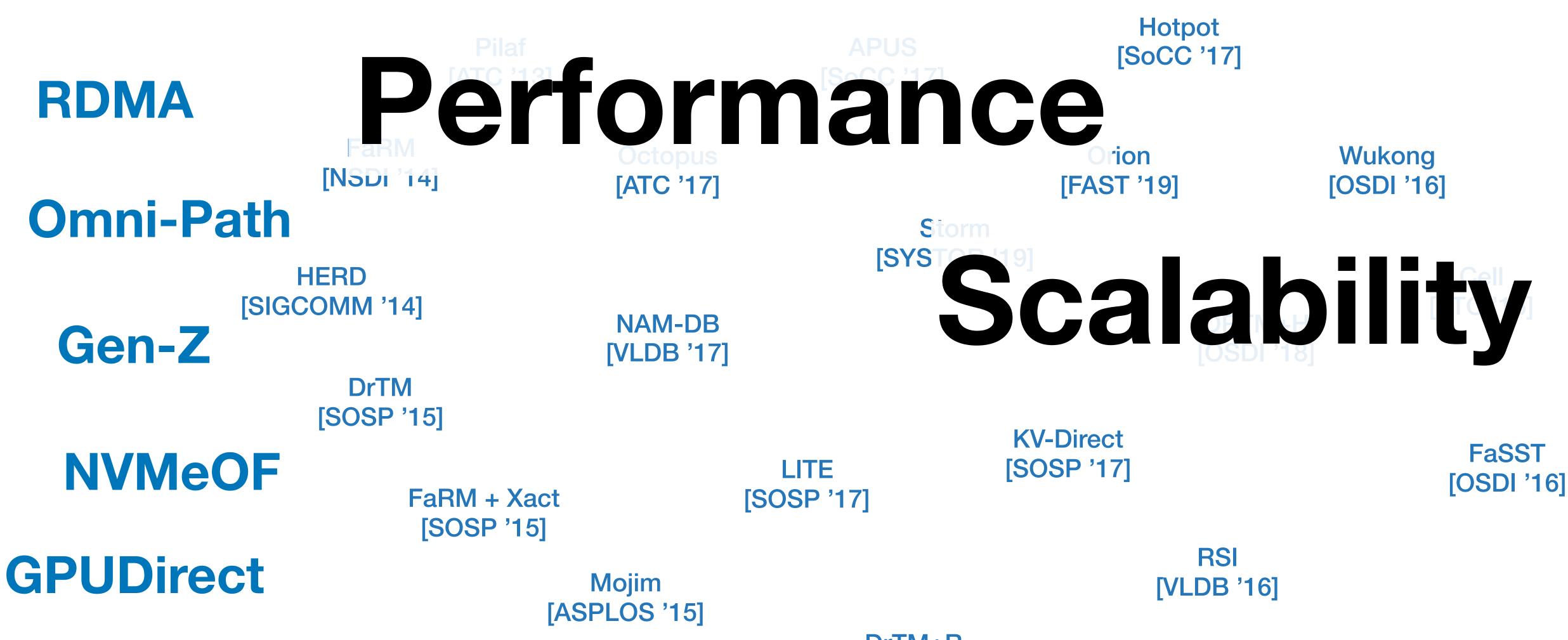


**FaSST** [OSDI '16]

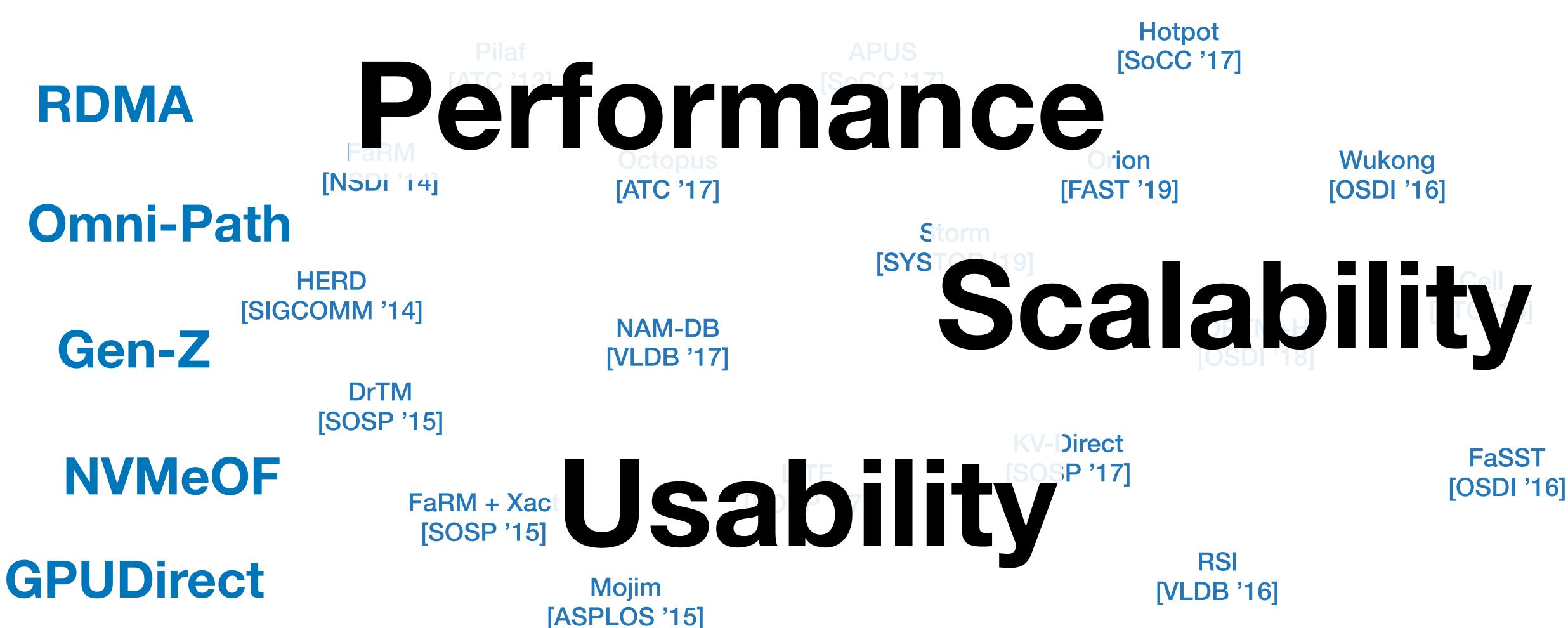




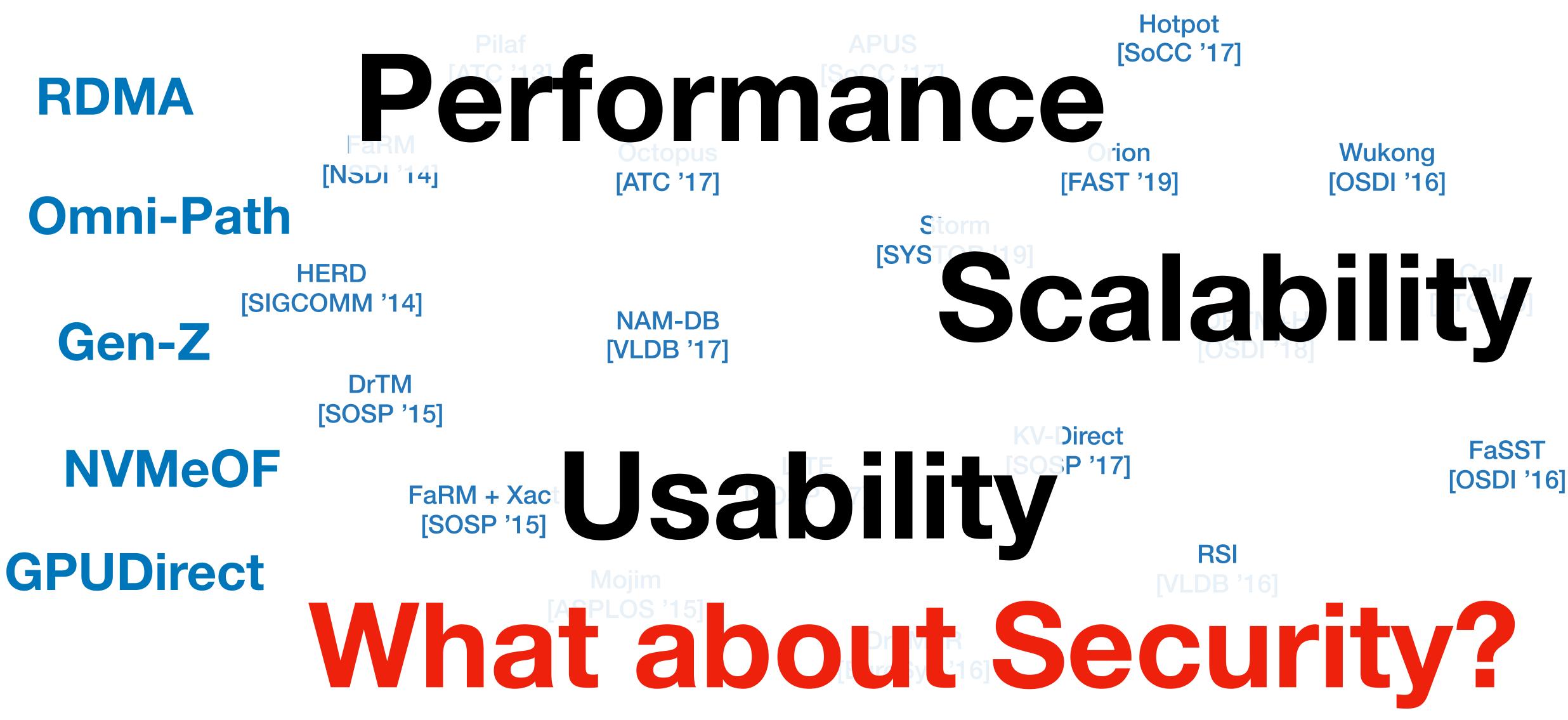




















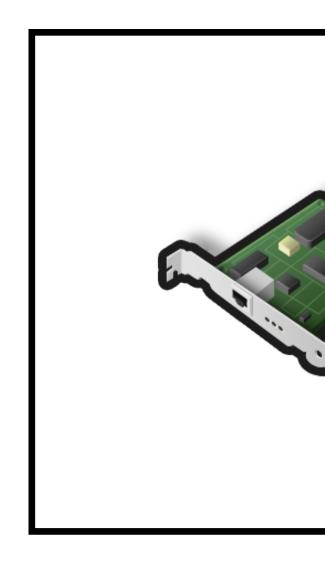
- Introduction and Background
- Vulnerabilities in One-Sided Communication
- Vulnerabilities in One-Sided Hardware
- Opportunities in One-Sided Communication
- Conclusion

# Outline



## • WRITE accountability





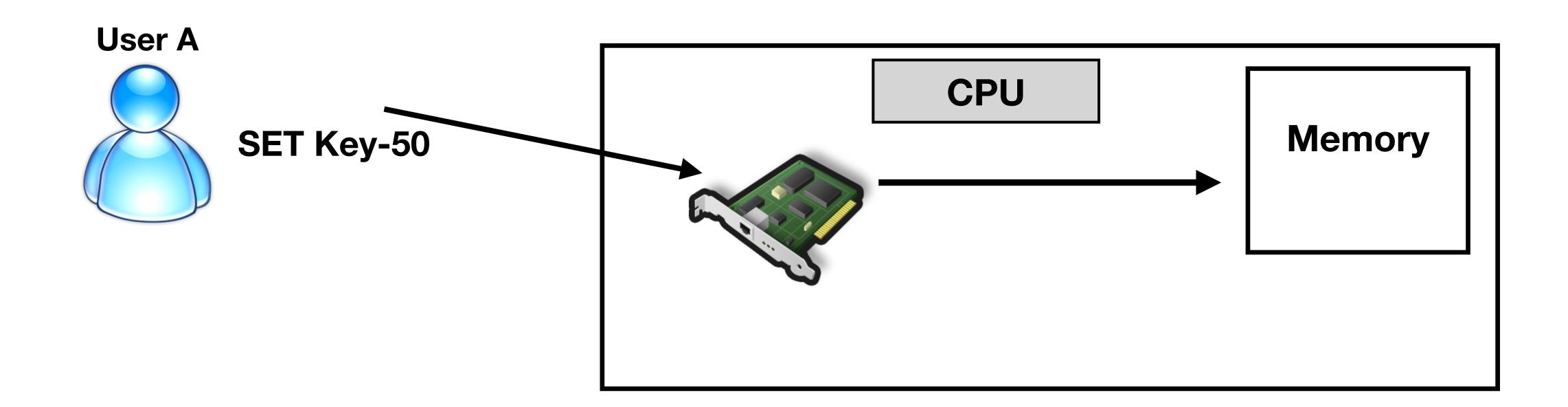
### CPU

Memory





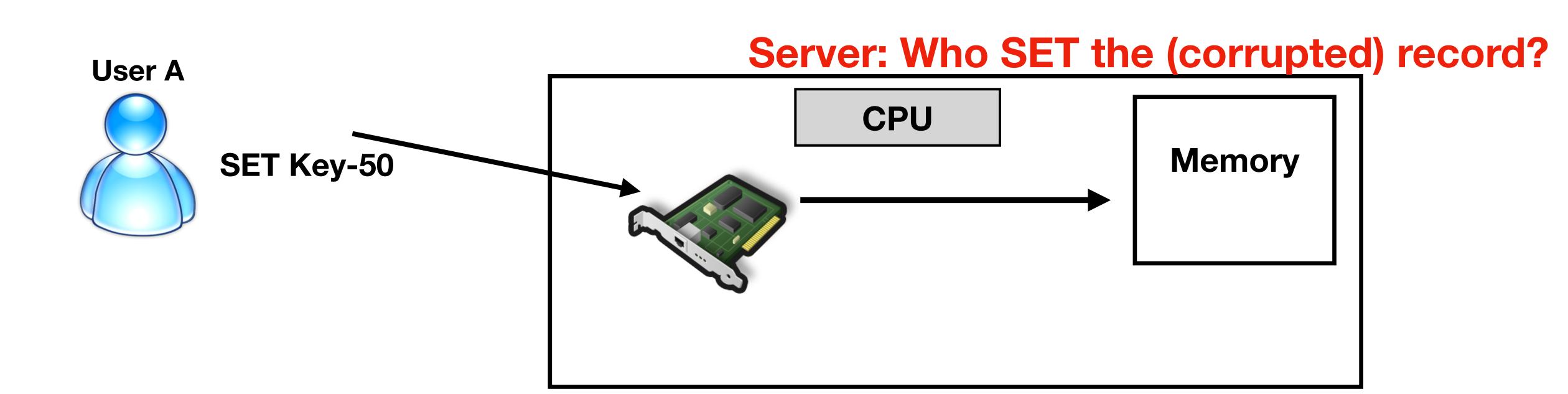
## • WRITE accountability







## WRITE accountability

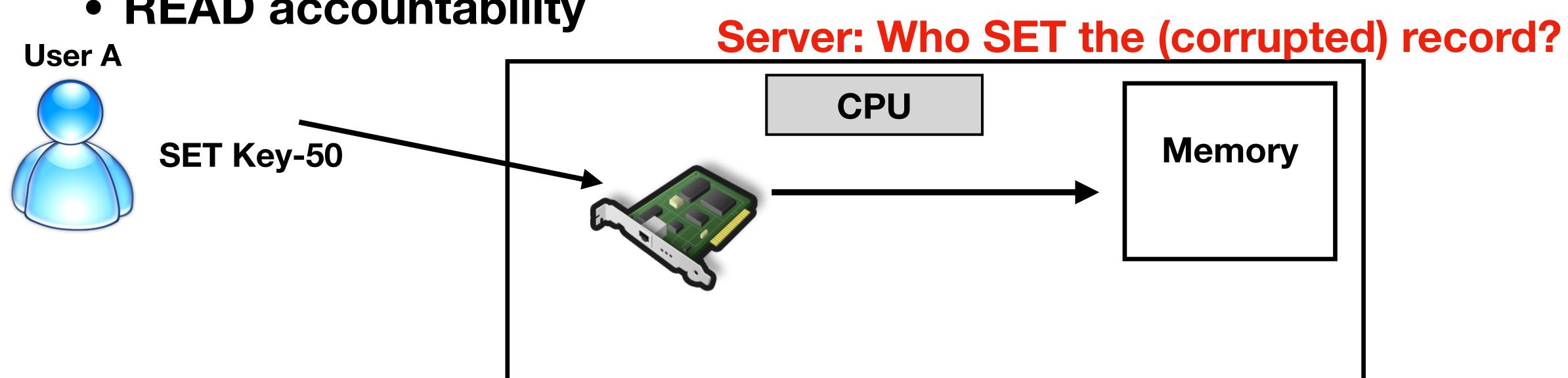






### WRITE accountability

### READ accountability

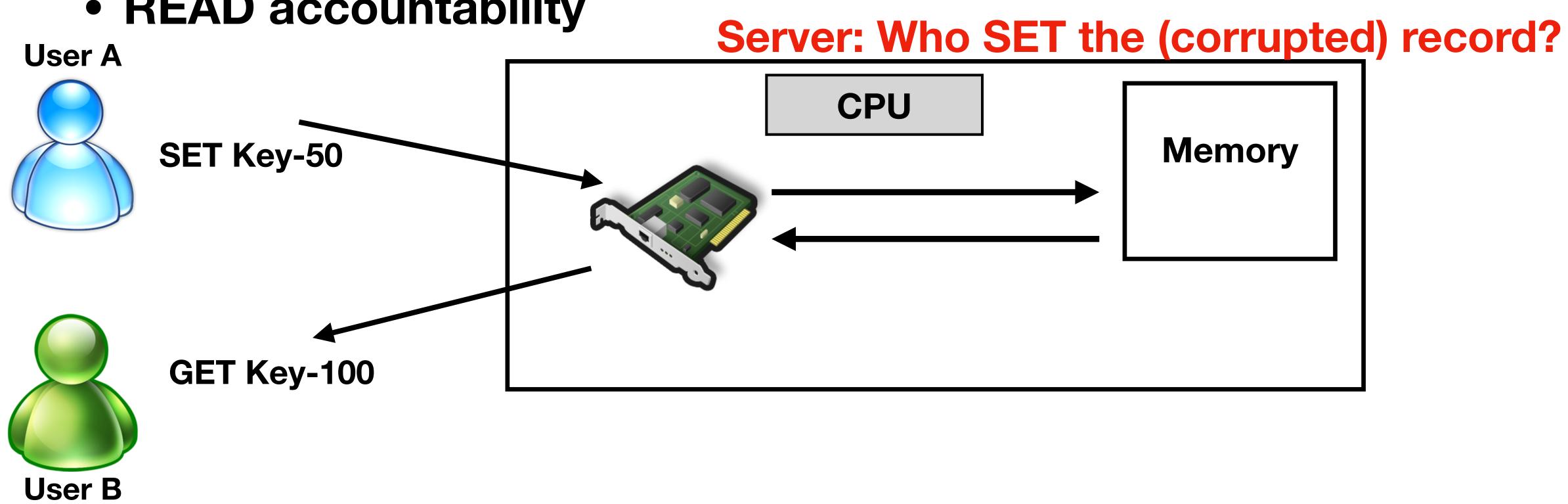






## WRITE accountability

## READ accountability

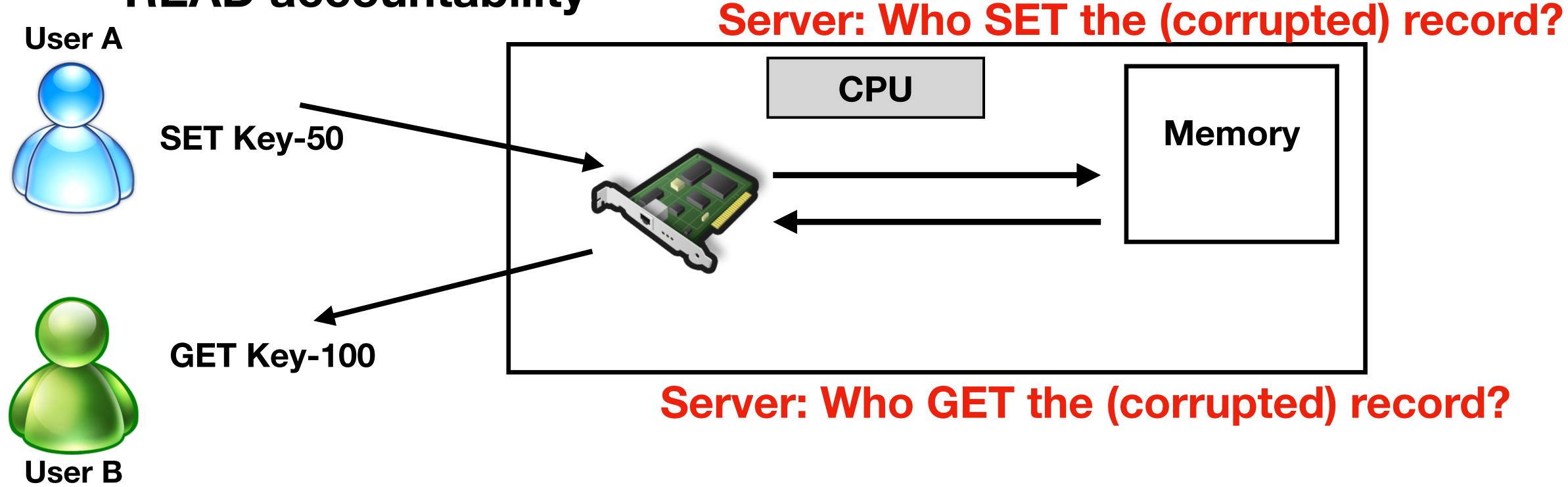






## WRITE accountability

## READ accountability

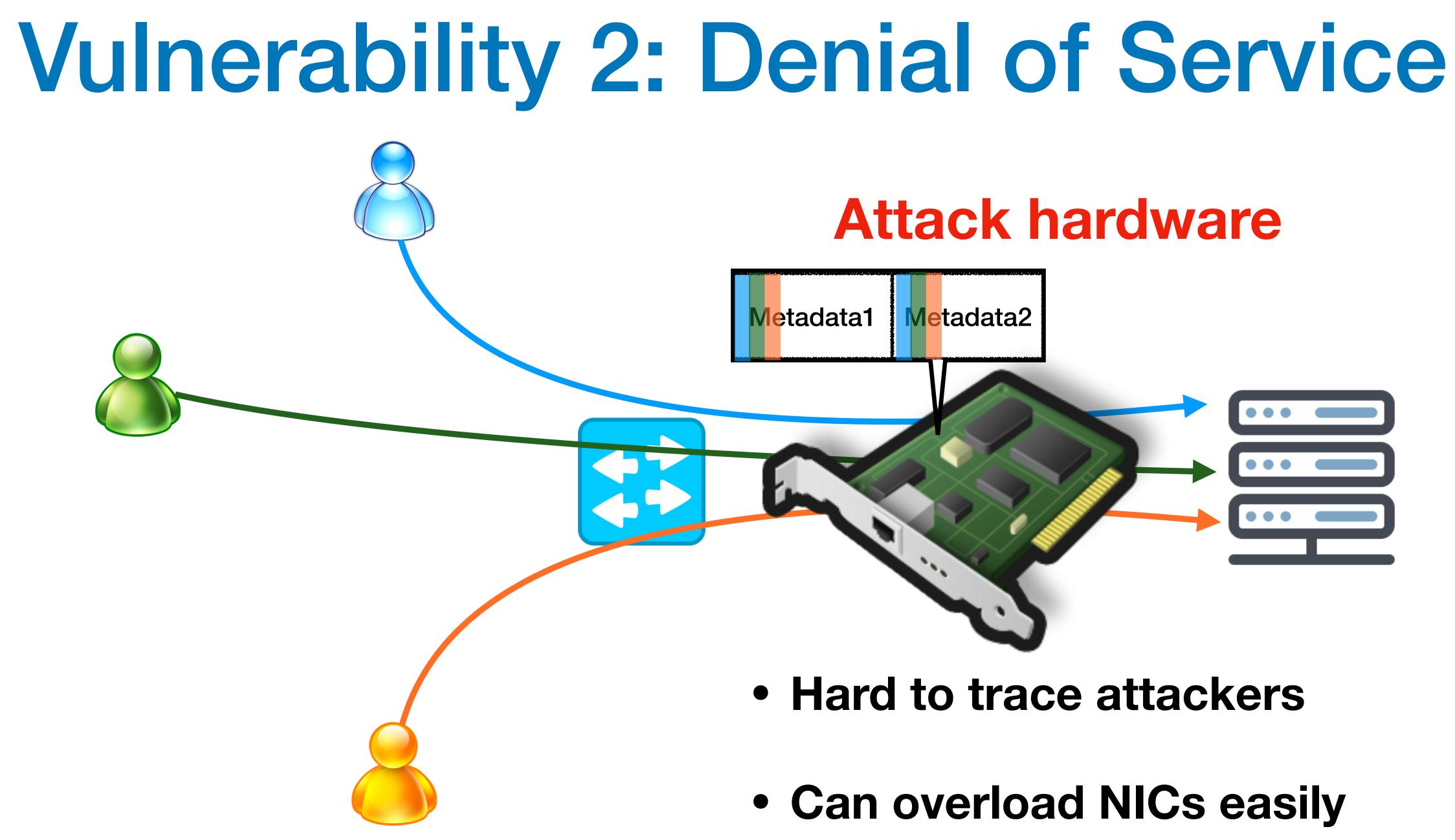




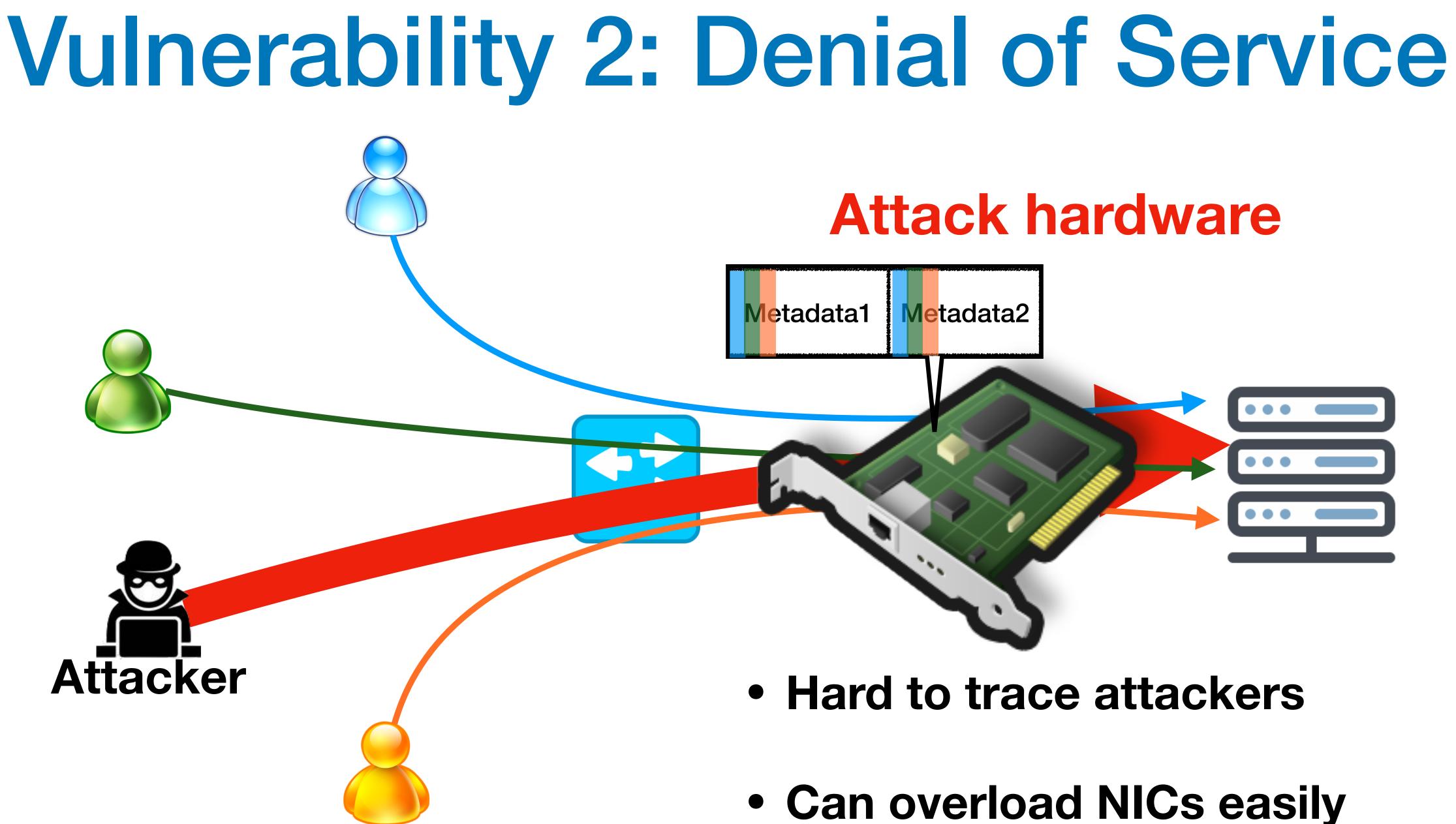




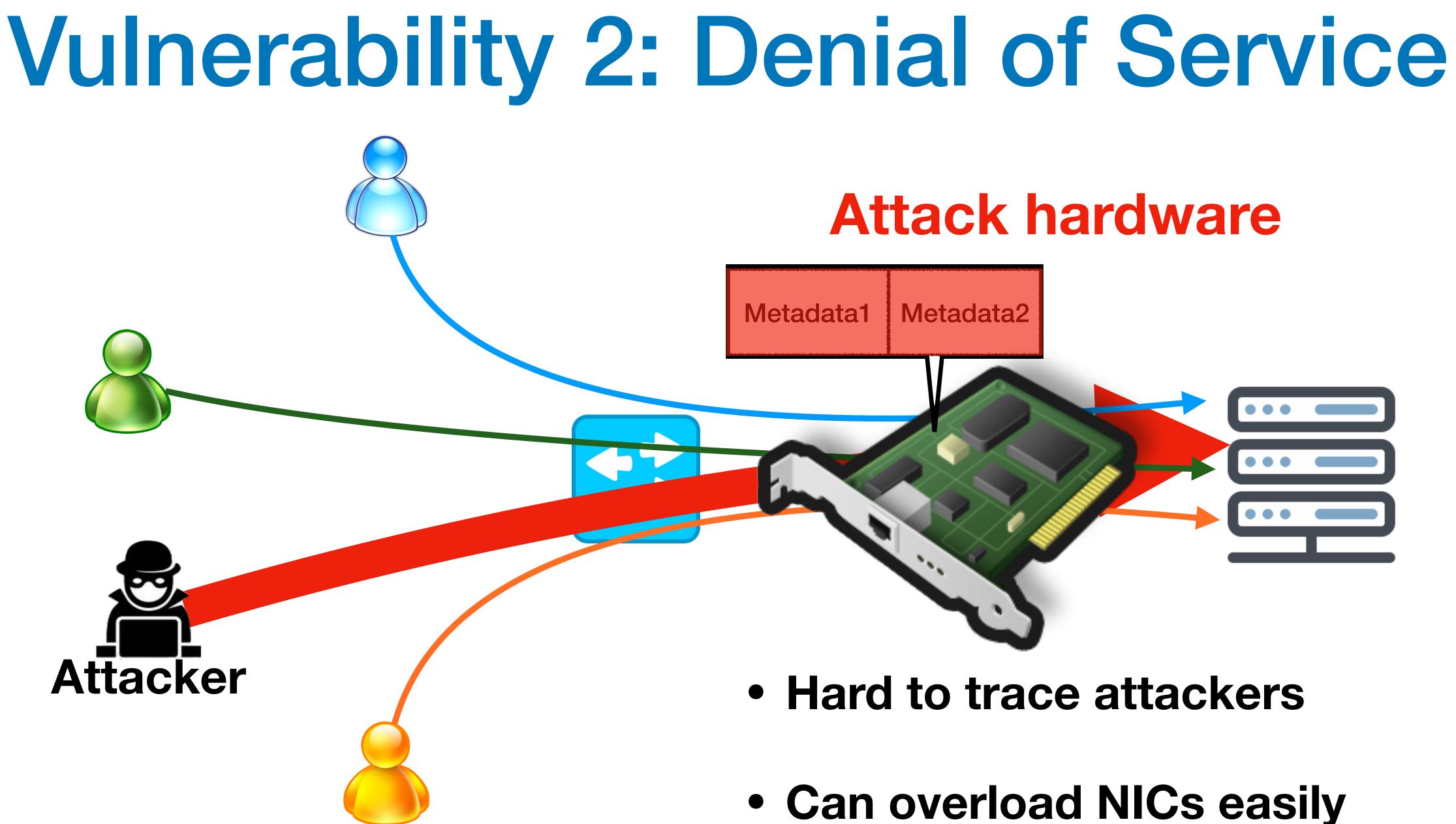




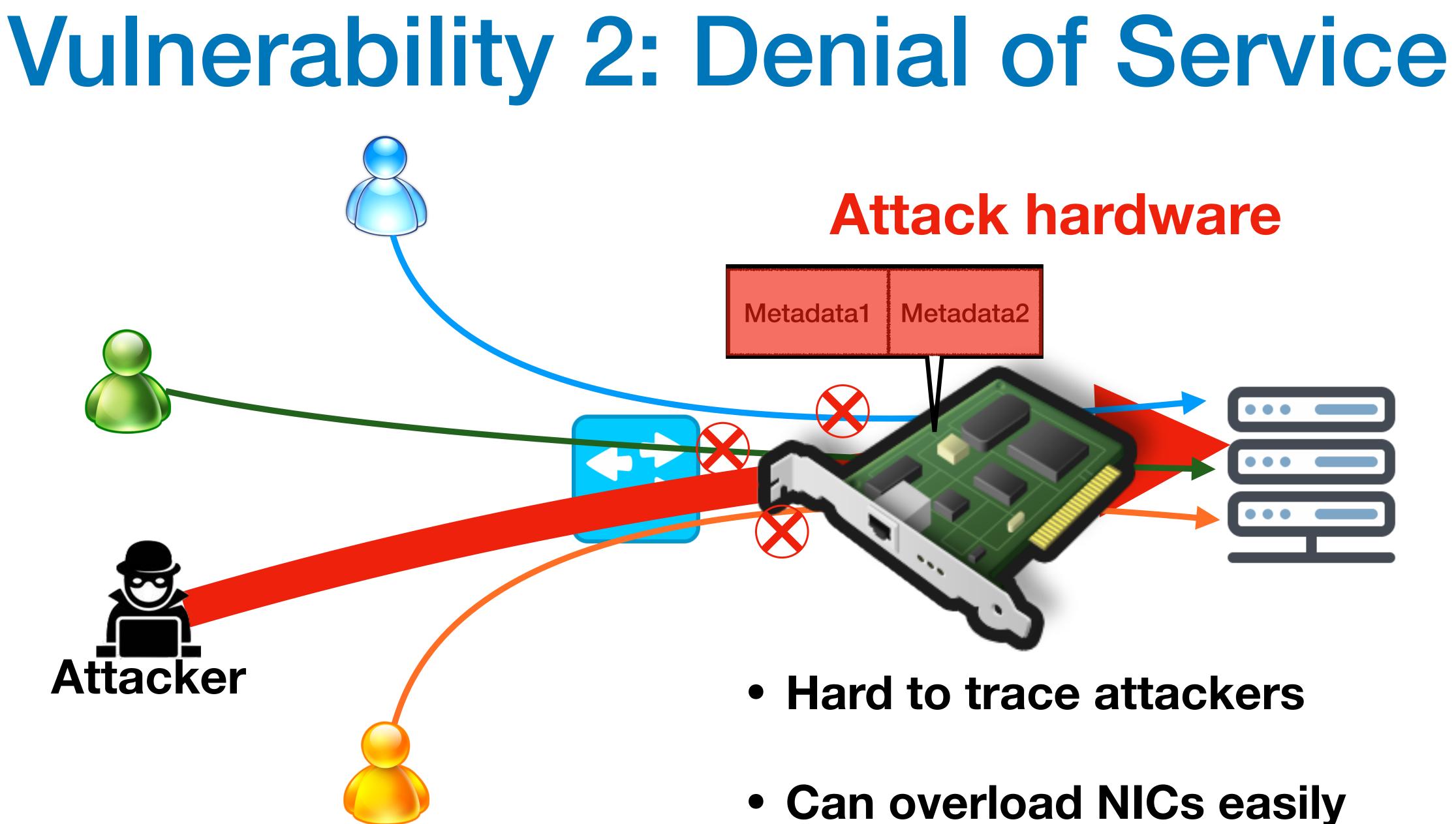








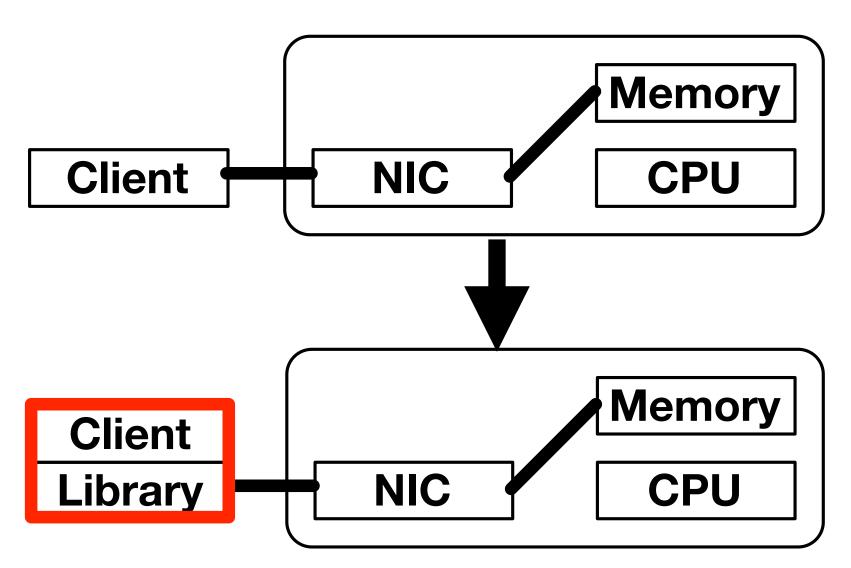






# **Discussion and Defense**

### **Intermediate Layer**



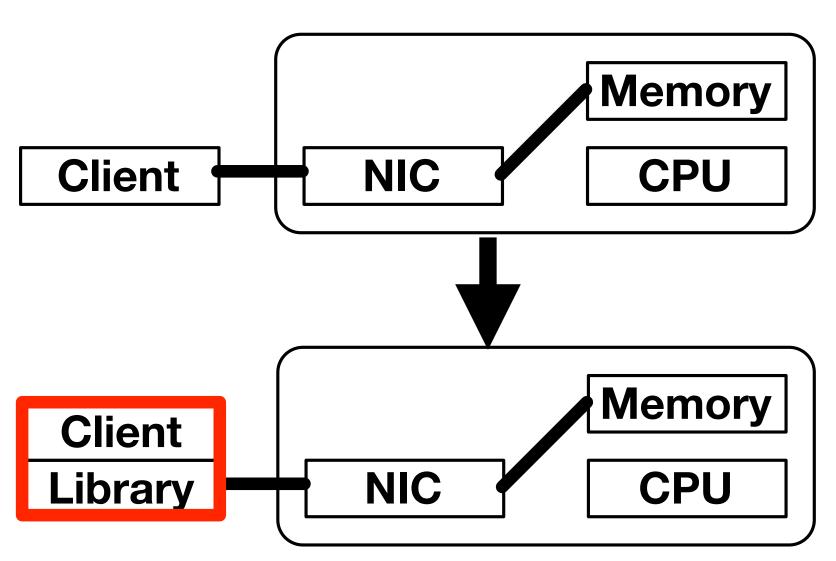
Adding intermediate layer at the sender side

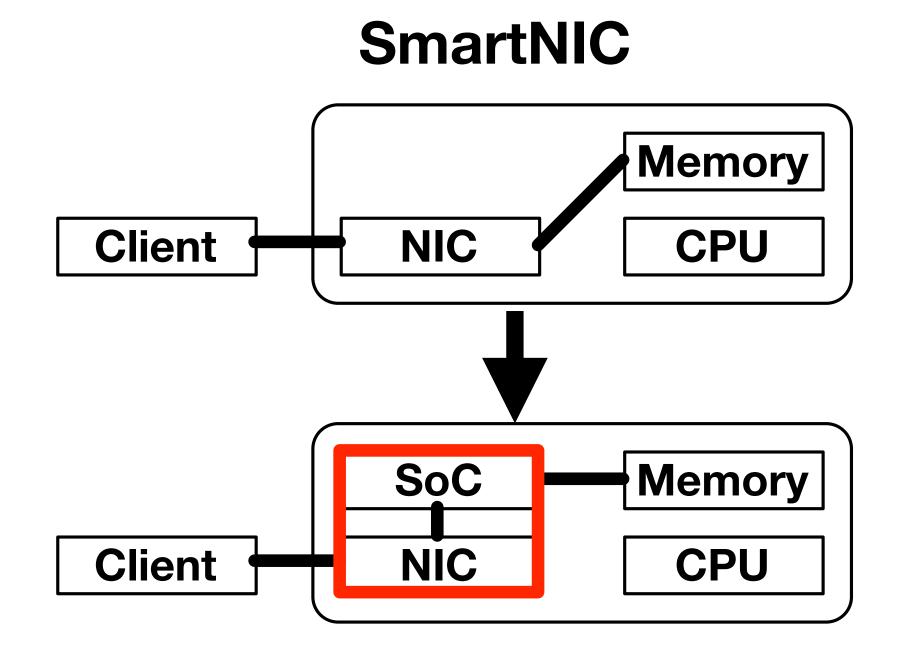


# **Discussion and Defense**

- Adding intermediate layer at the sender side
- Enhancing SmartNIC at the receiver side

### **Intermediate Layer**





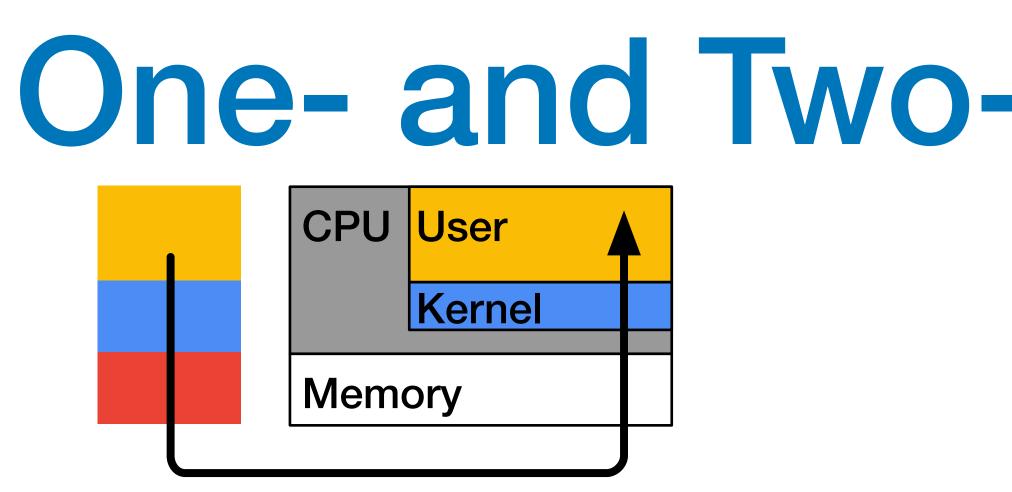




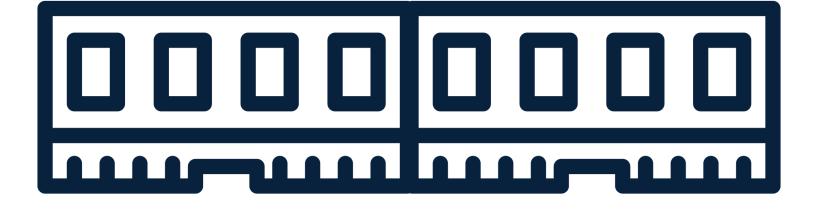
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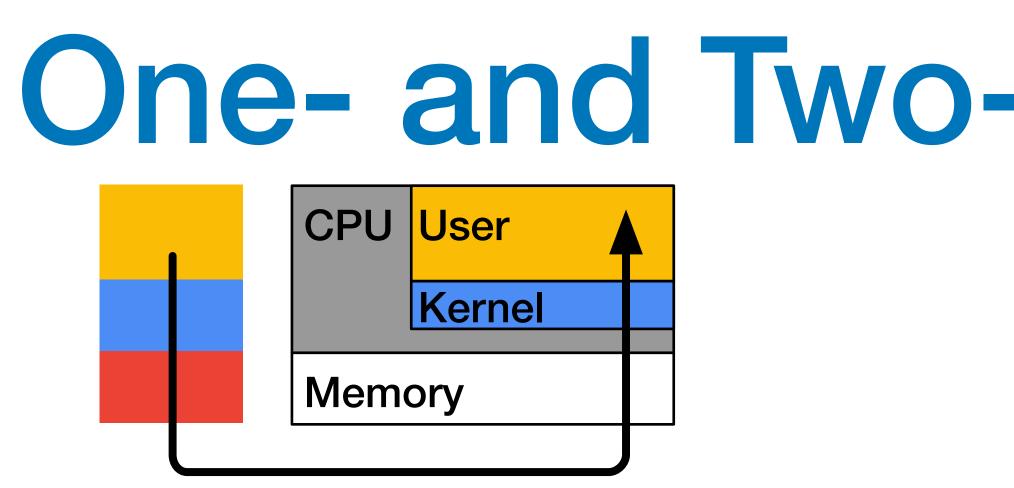


**Two-Sided** 



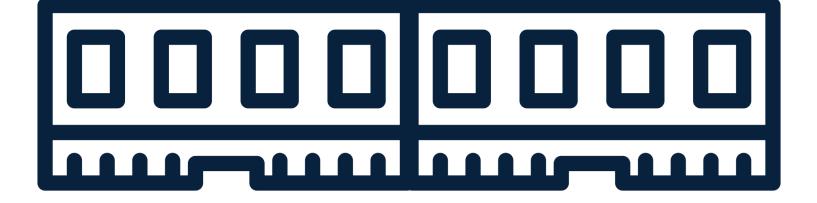
# **One- and Two-Sided Hardware**





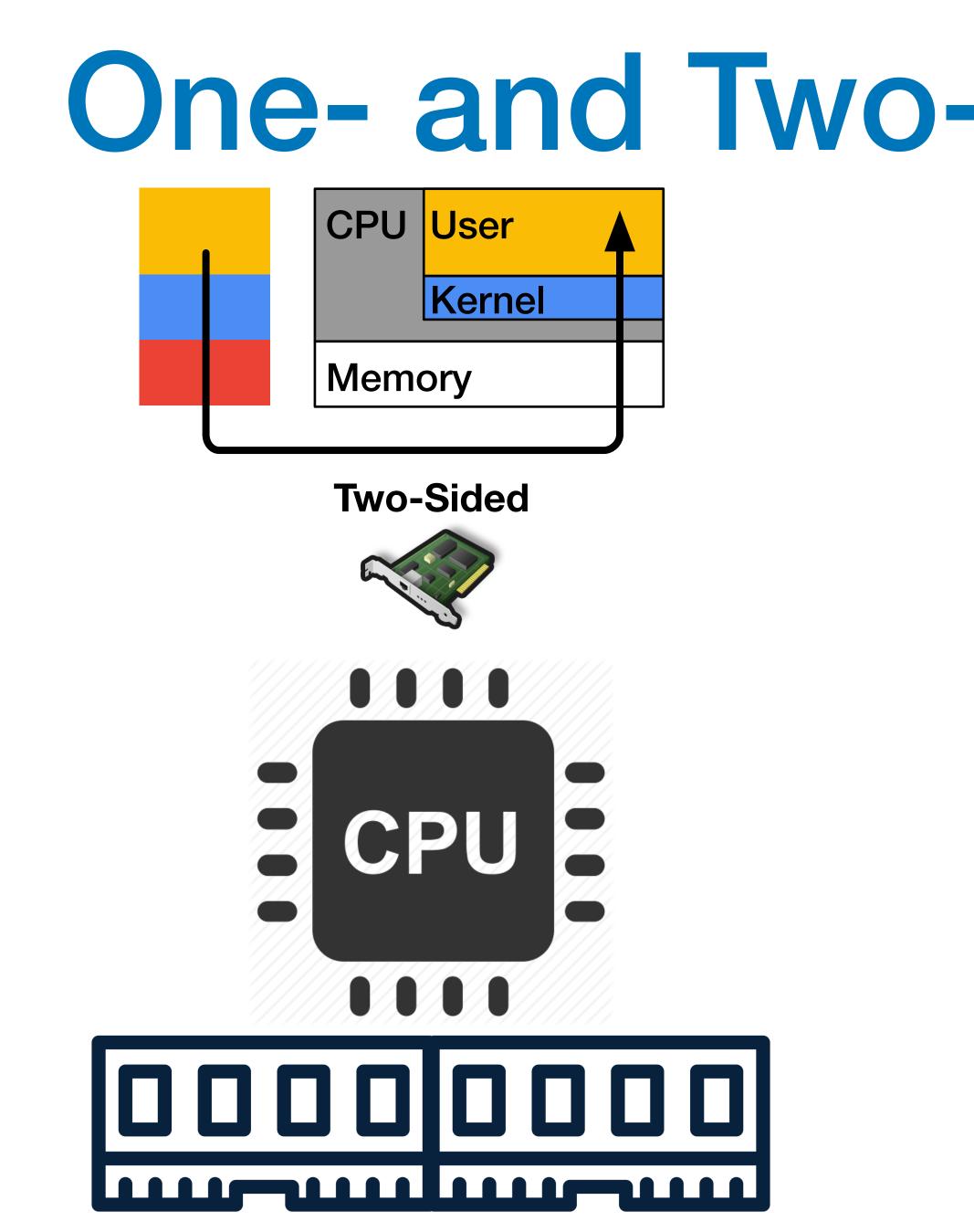
**Two-Sided** 





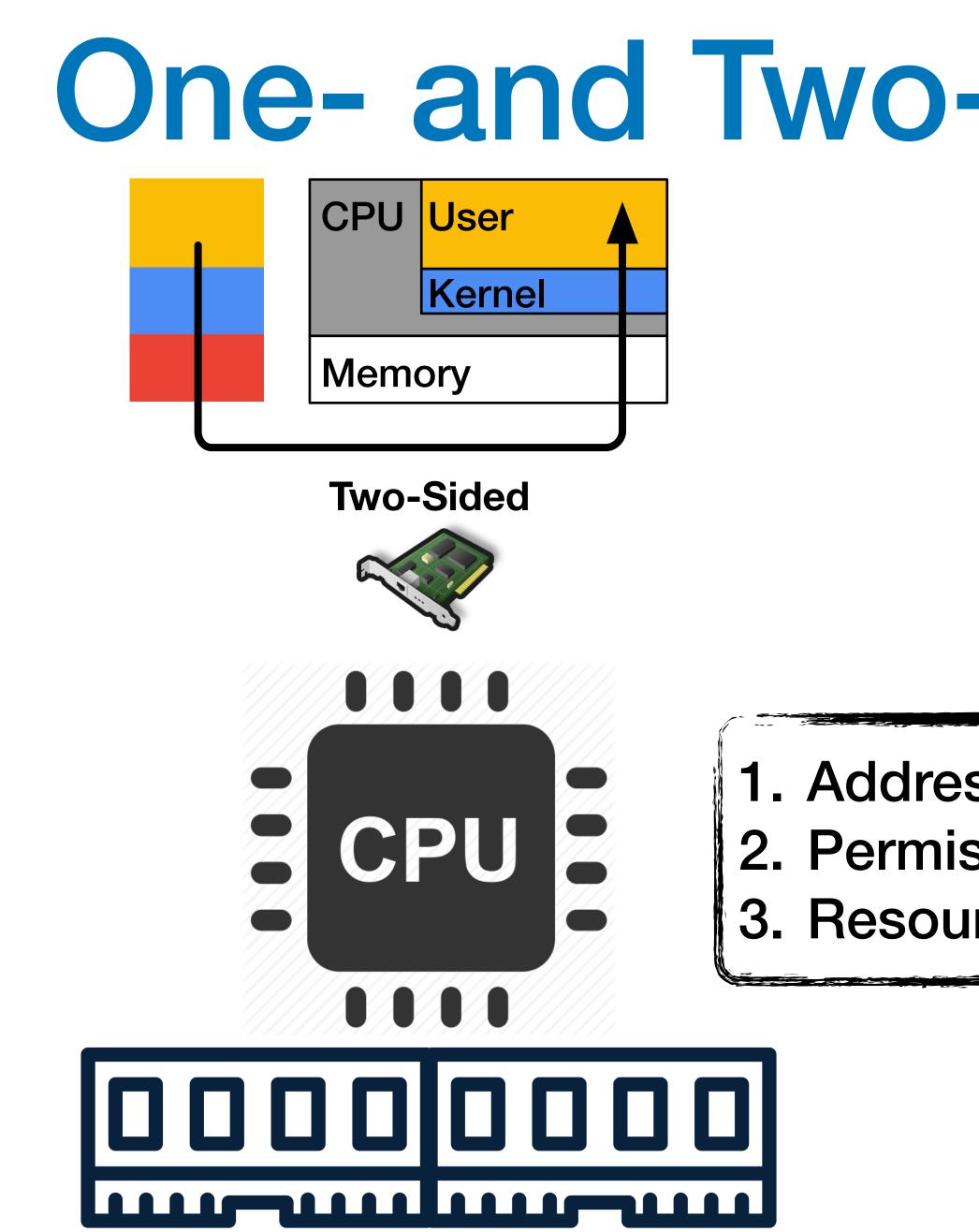
# **One- and Two-Sided Hardware**





## **One- and Two-Sided Hardware**

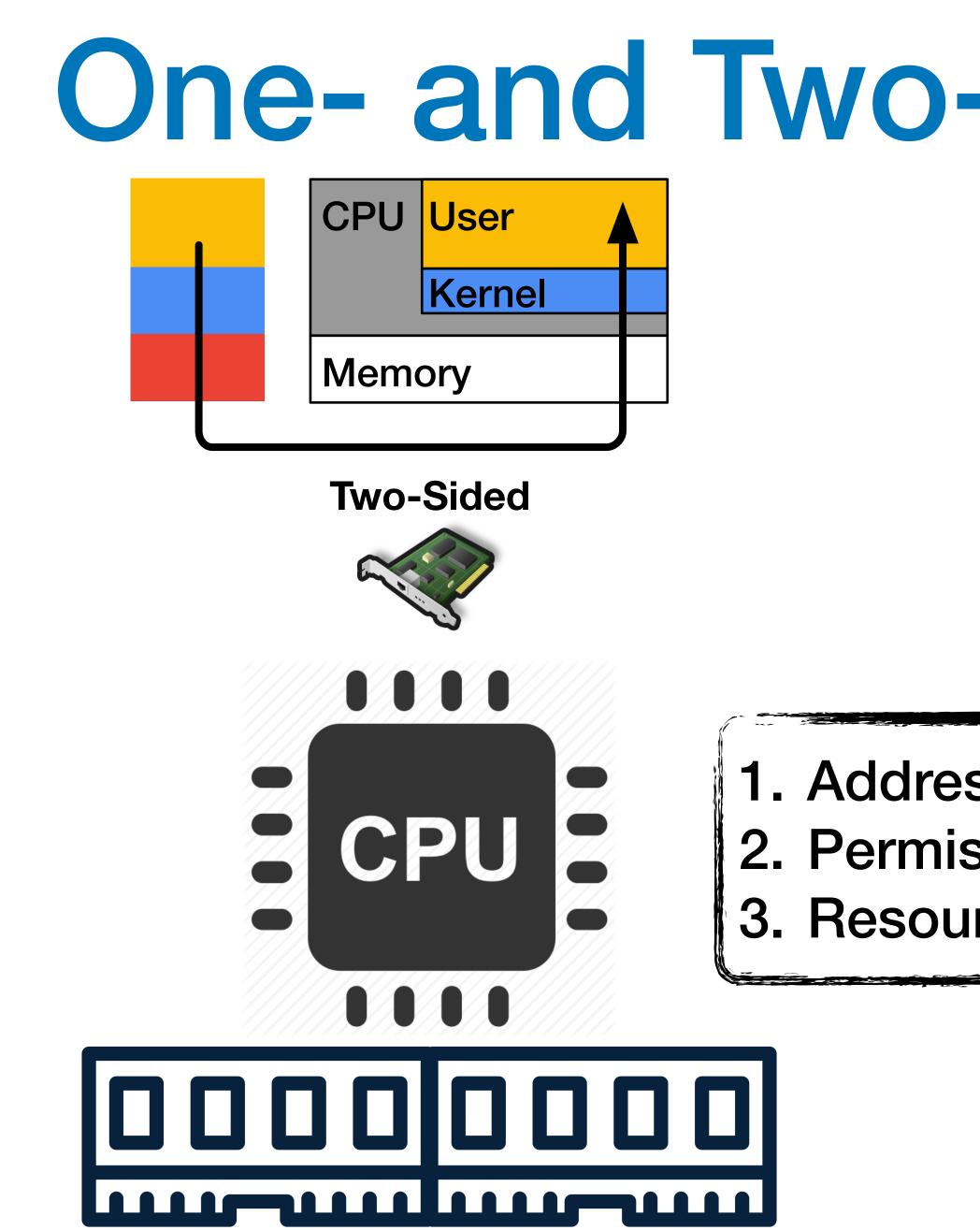




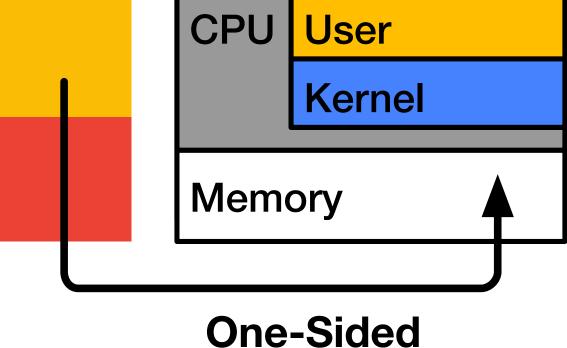
## **One- and Two-Sided Hardware**

Address mapping
Permission checking
Resource isolation



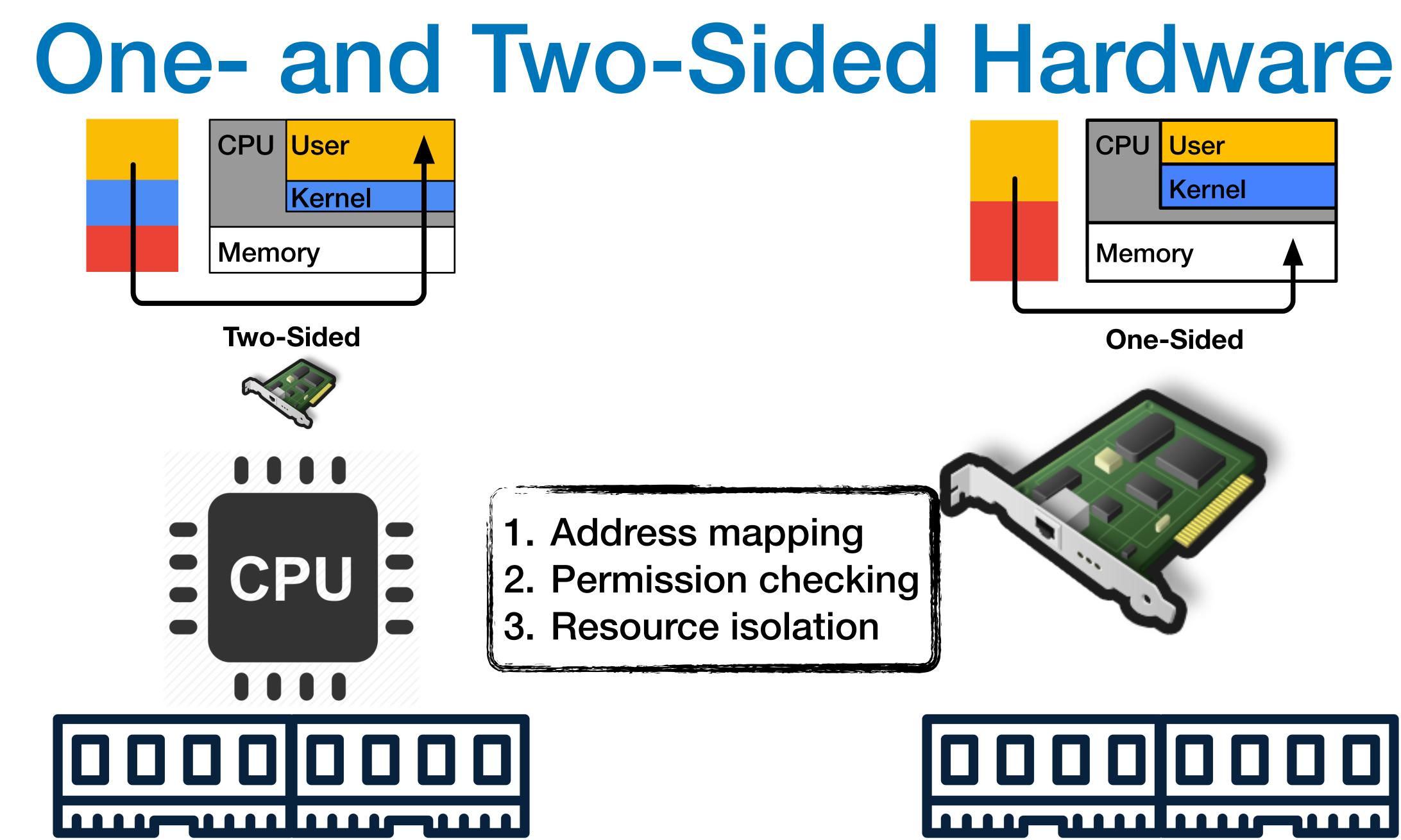


# One- and Two-Sided Hardware

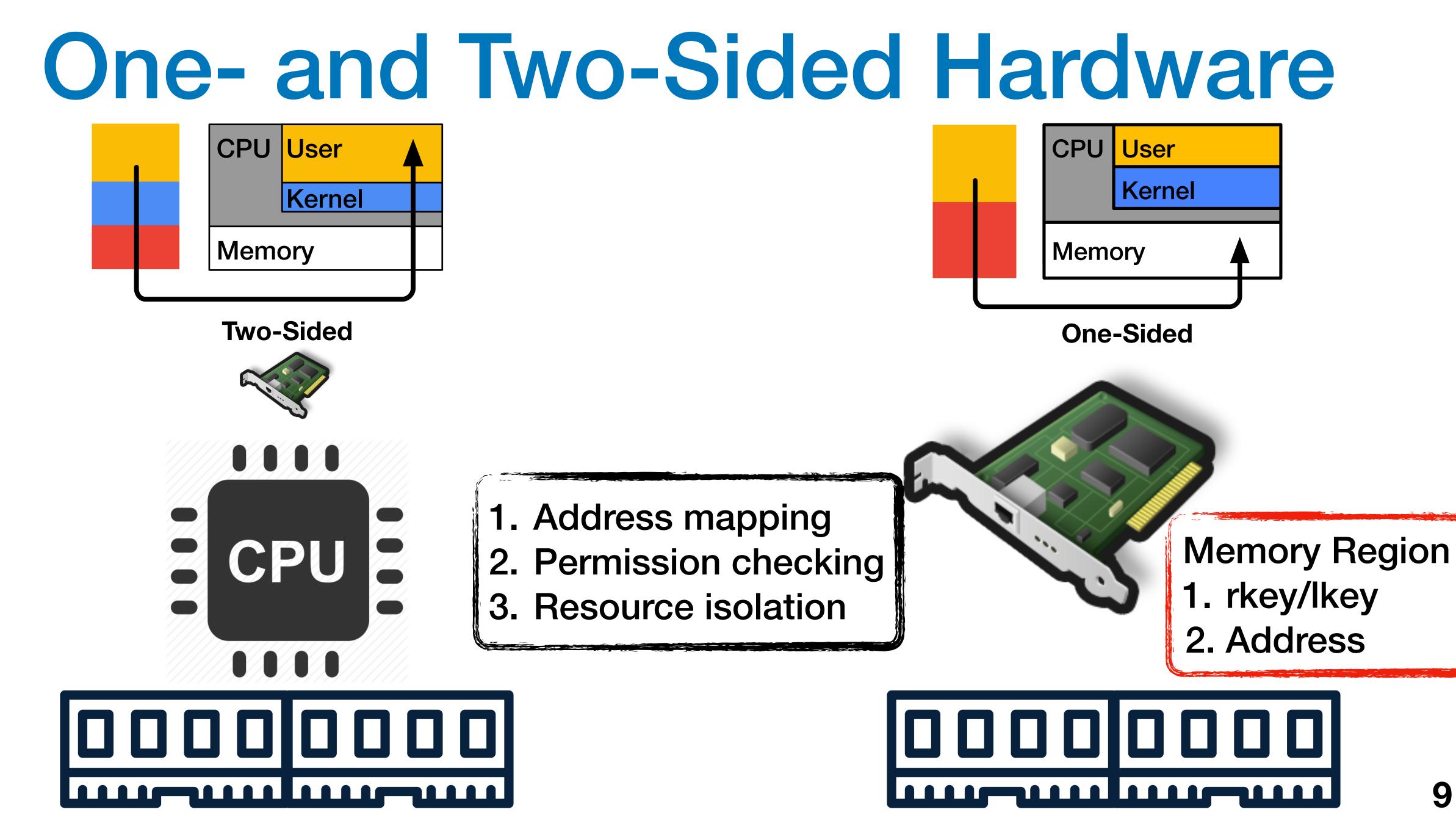


Address mapping
Permission checking
Resource isolation



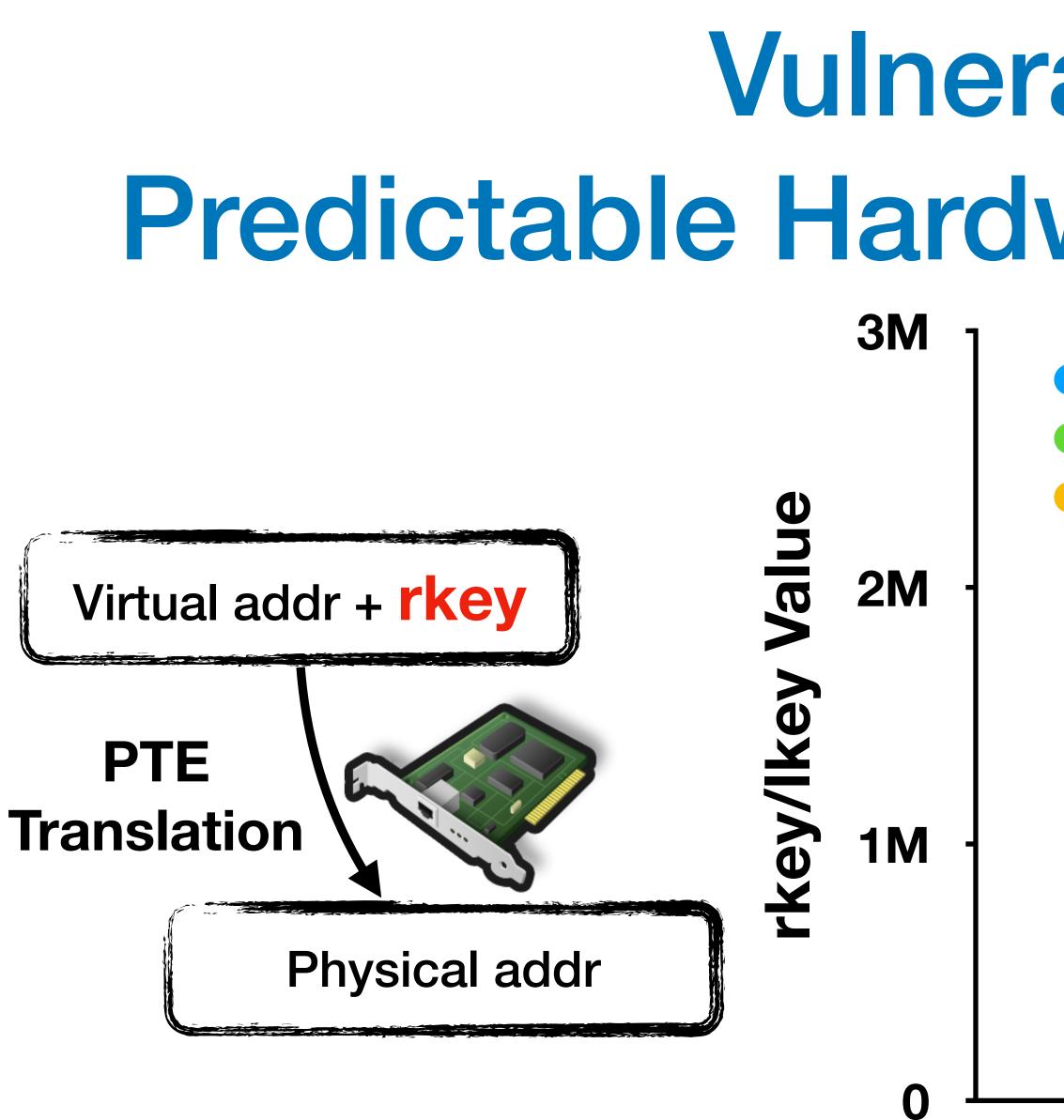












### Vulnerability 3 -**Predictable Hardware Managed Keys**

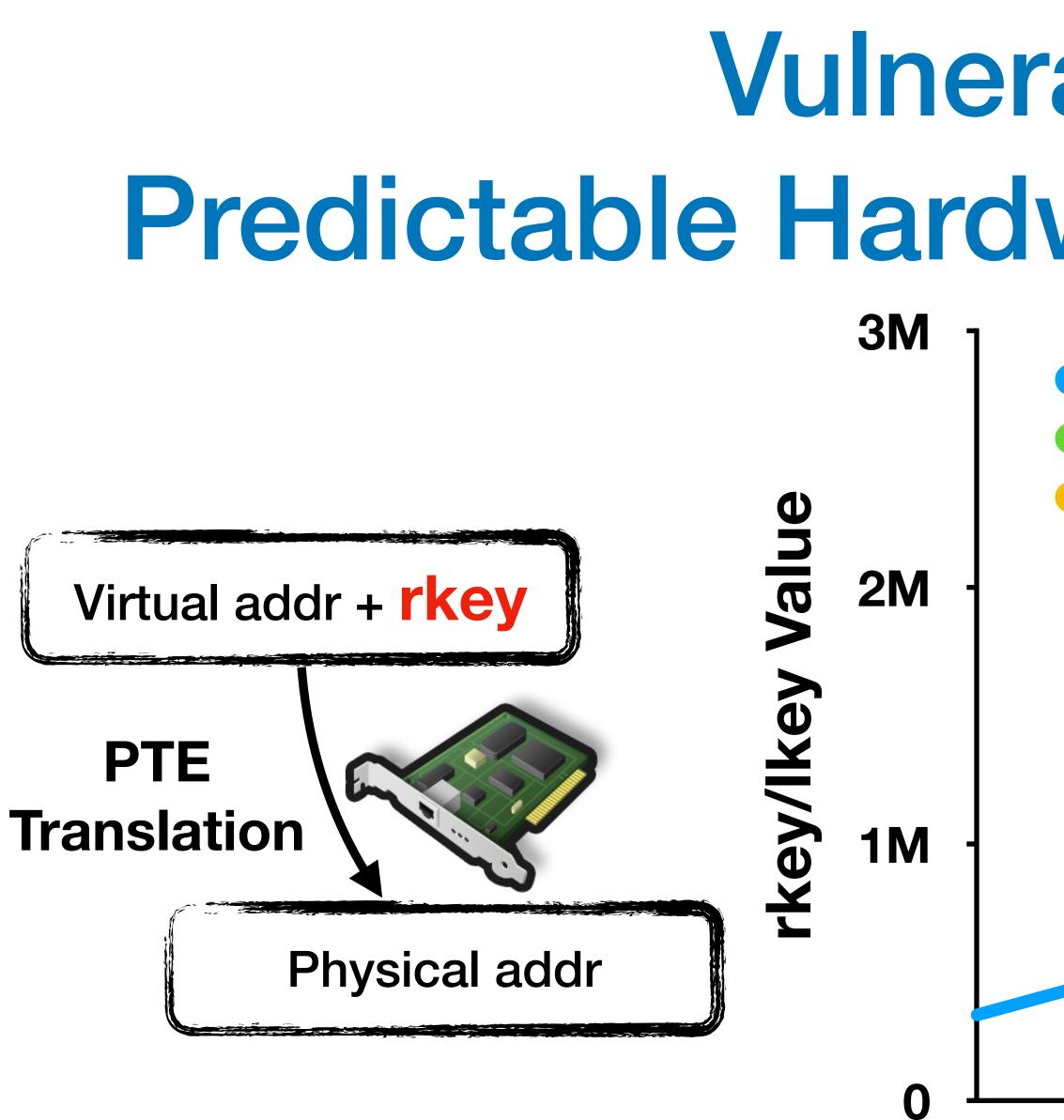
- ConnectX-3
- ConnectX-4
- ConnectX-5

0

#### 1000 2000 3000 4000 5000 nth-MemoryRegion Registered







### Vulnerability 3 -**Predictable Hardware Managed Keys**

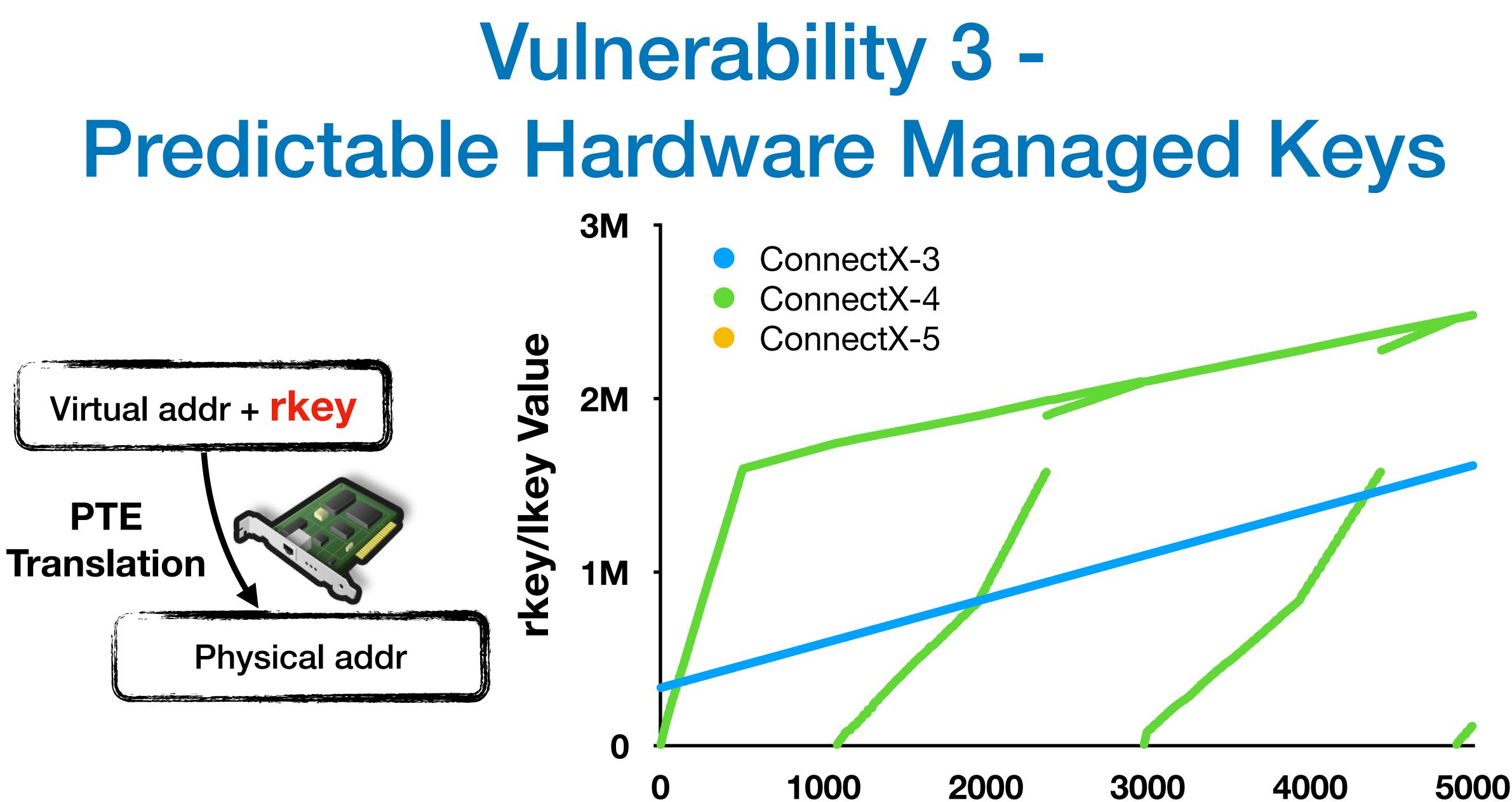
- ConnectX-3
- ConnectX-4
- ConnectX-5

0

#### 1000 2000 3000 4000 5000 nth-MemoryRegion Registered



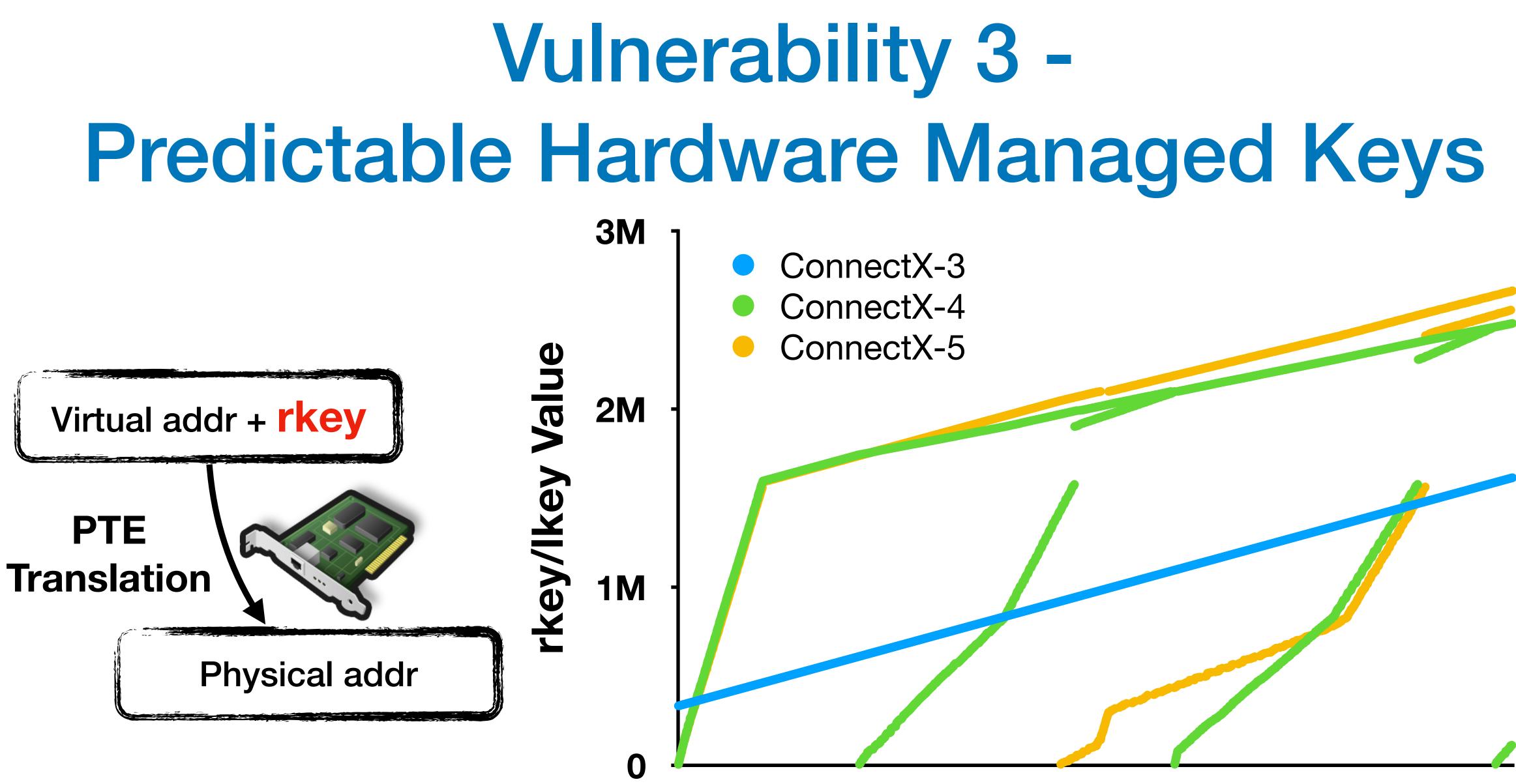




### nth-MemoryRegion Registered







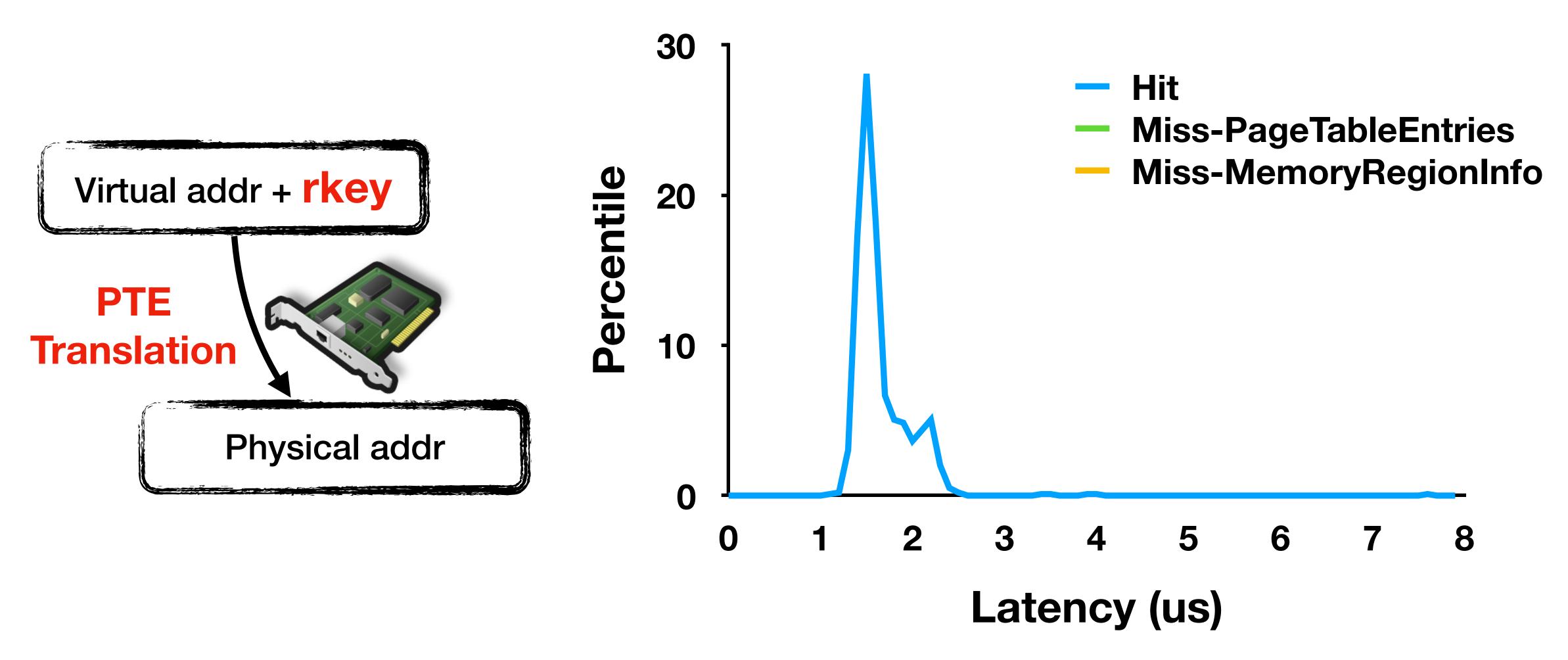
### nth-MemoryRegion Registered





# **Vulnerability 4 - Side Channel in NICs**

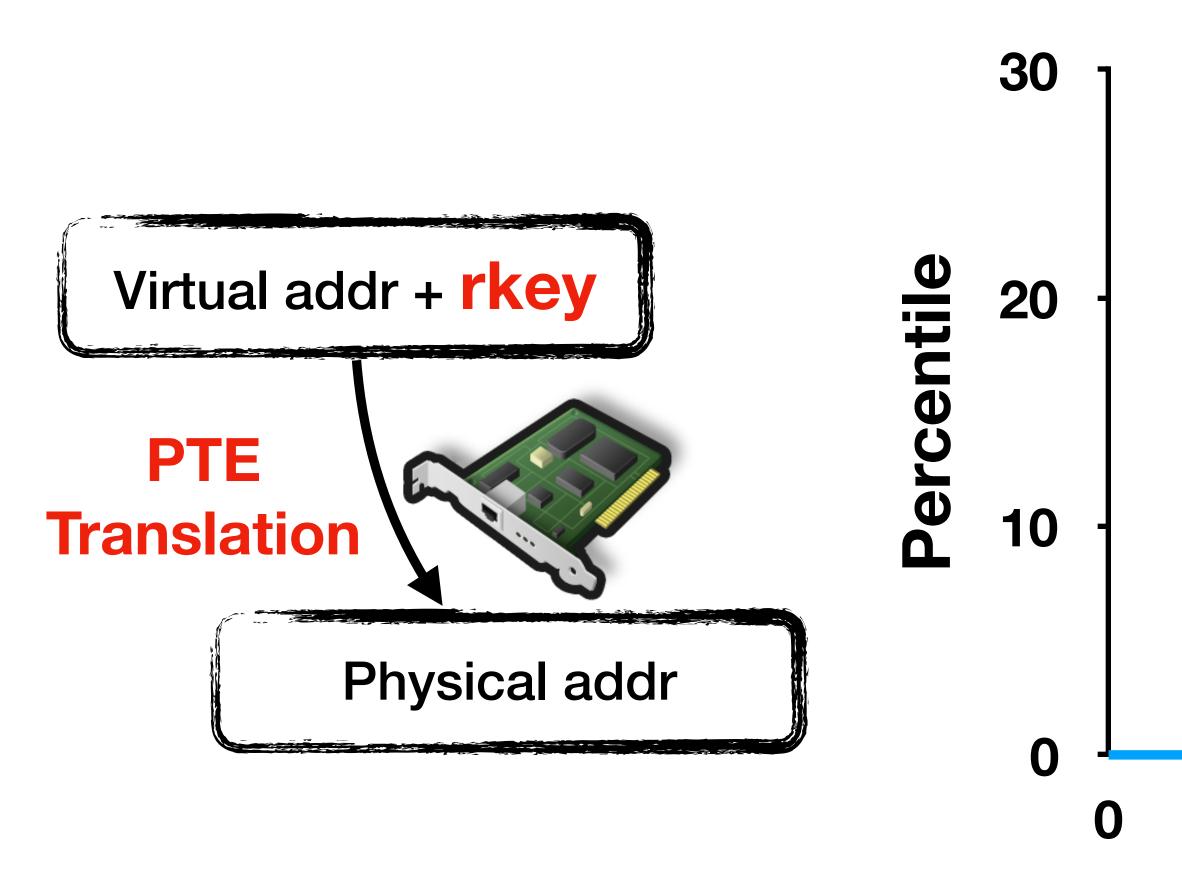
### **ConnectX-5, 1KB READ request latency**

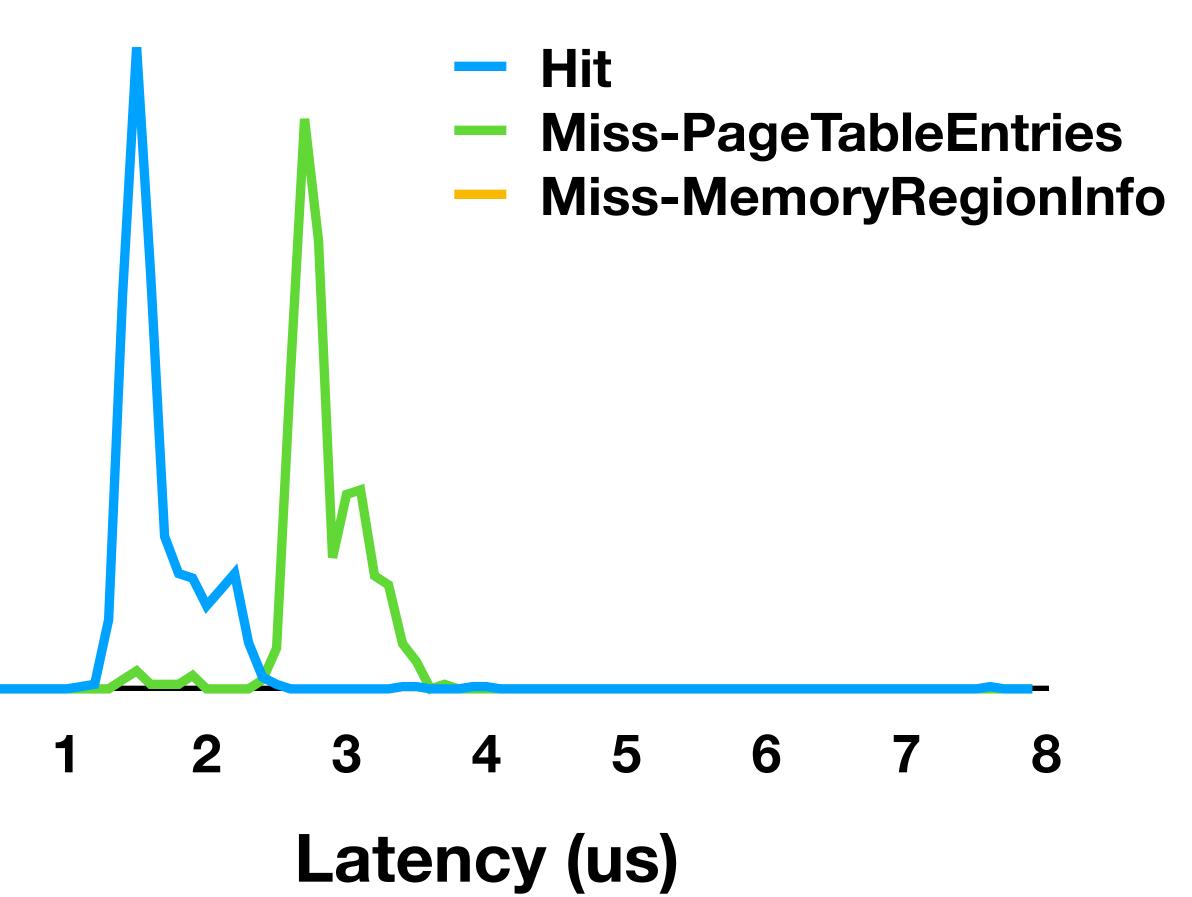




# **Vulnerability 4 - Side Channel in NICs**

### **ConnectX-5, 1KB READ request latency**

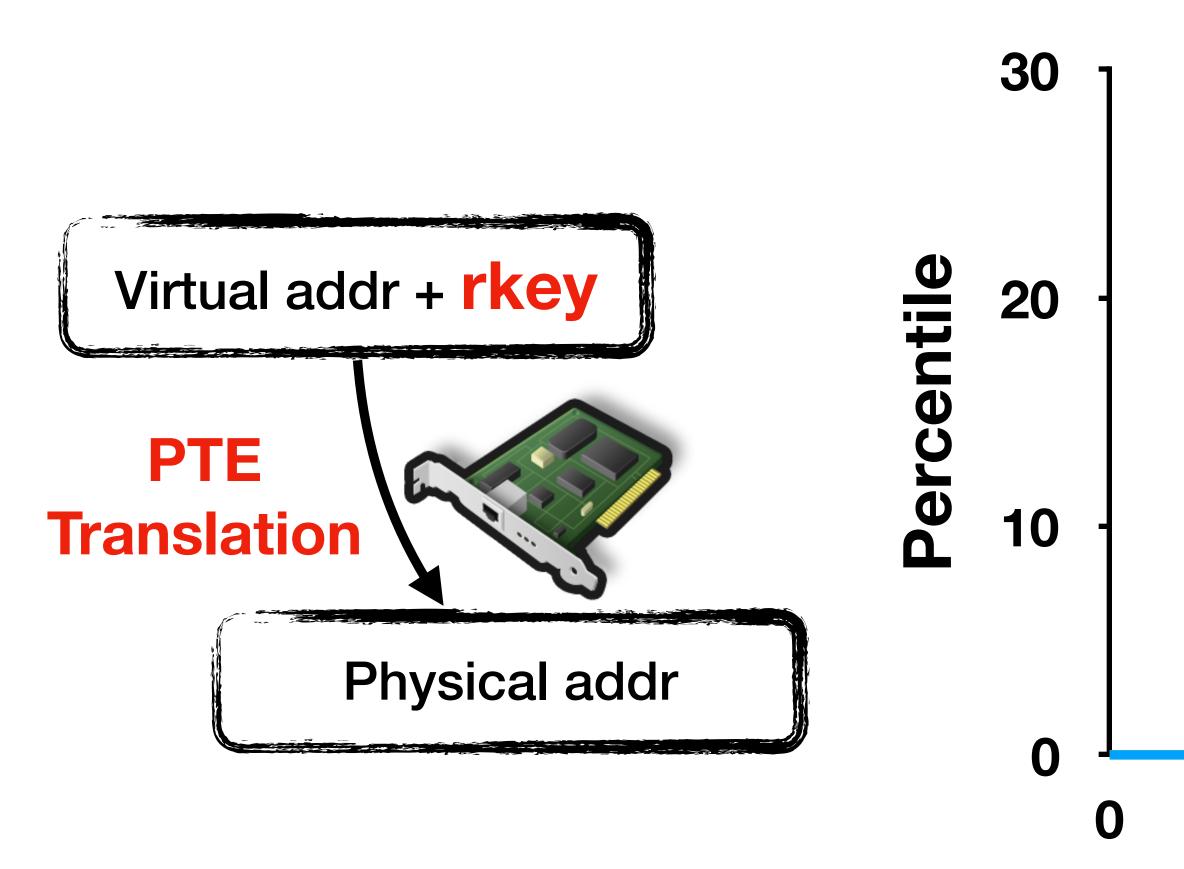


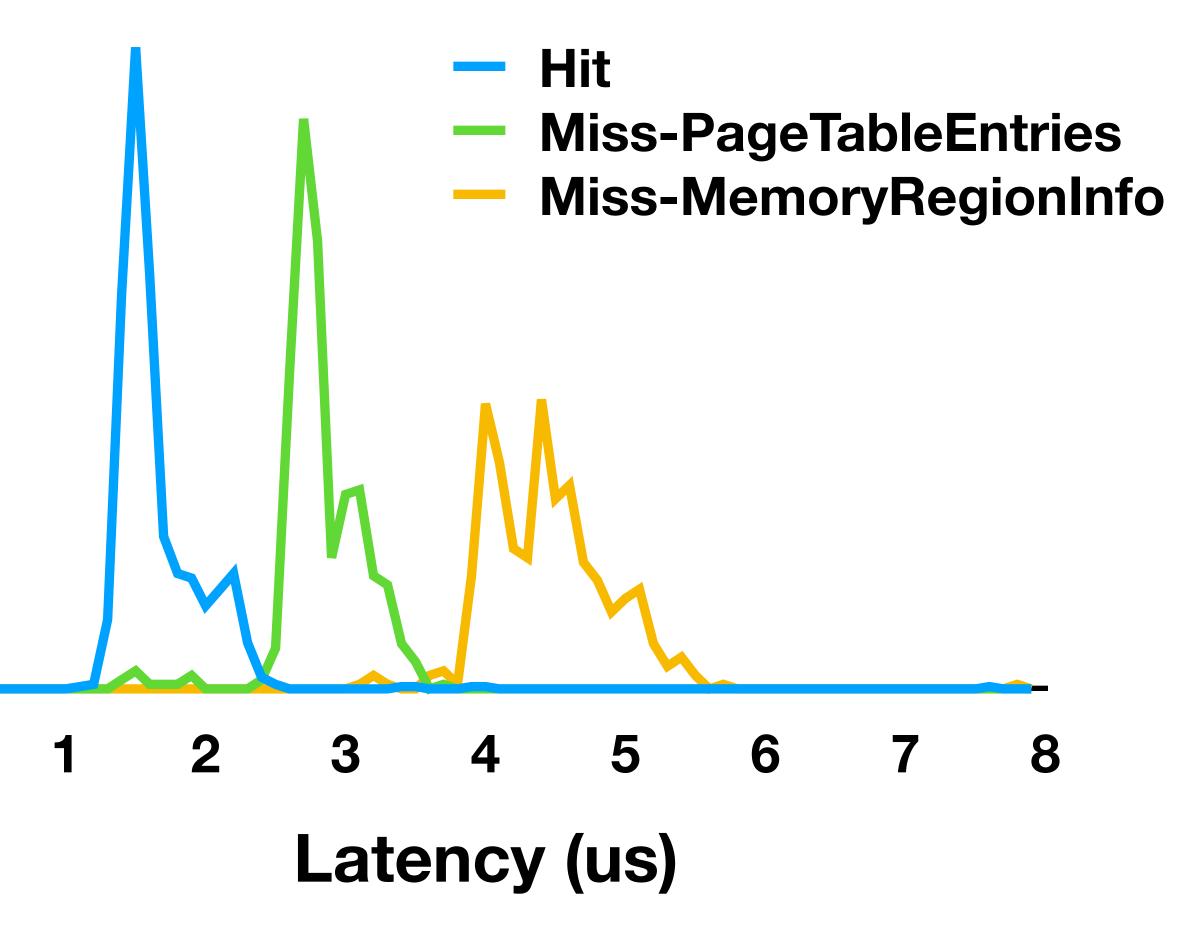




# **Vulnerability 4 - Side Channel in NICs**

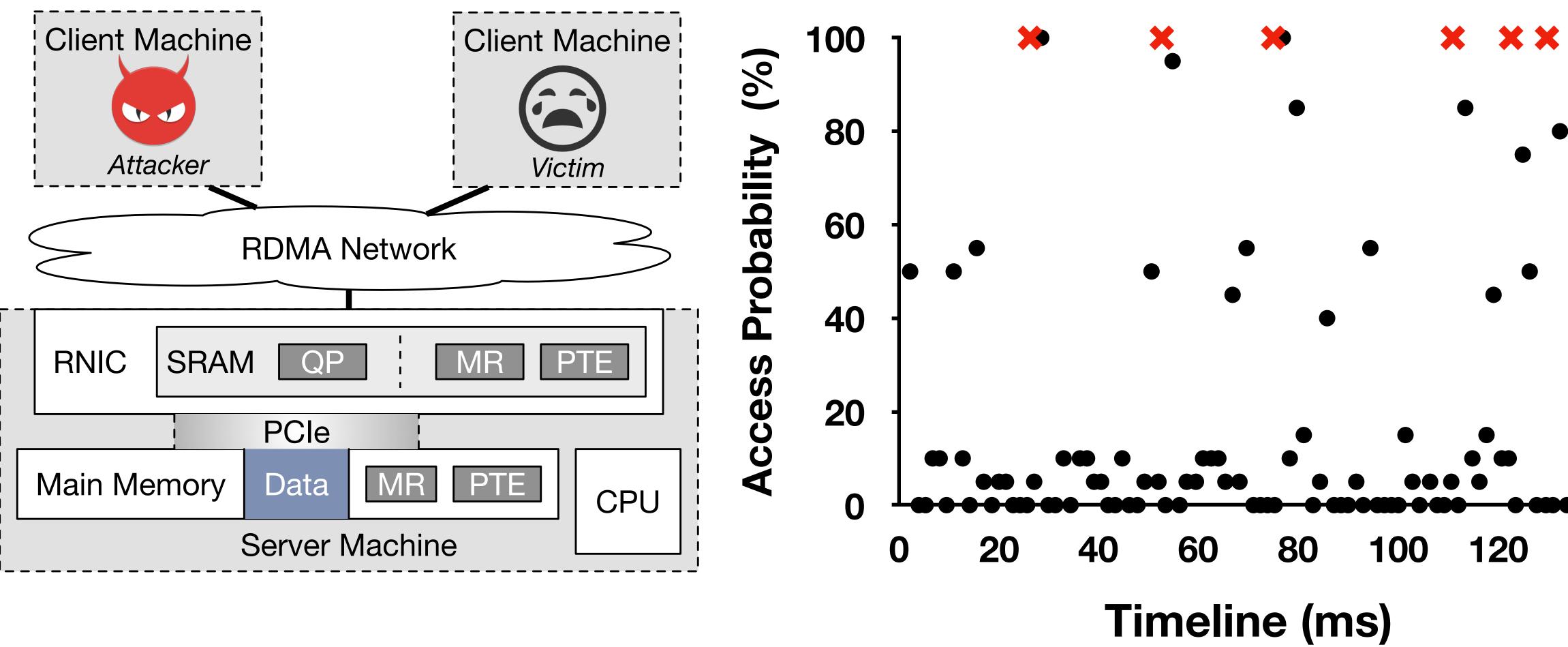
### **ConnectX-5, 1KB READ request latency**







## Side-Channel Attacks in RDMA (Pythia, USENIX Sec '19)





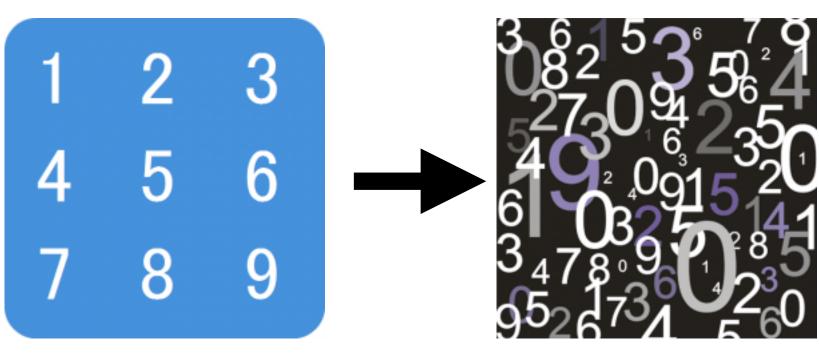




## **Discussion and Defense**

### Generate memory registration keys cryptographically

#### **Sequential to Random**

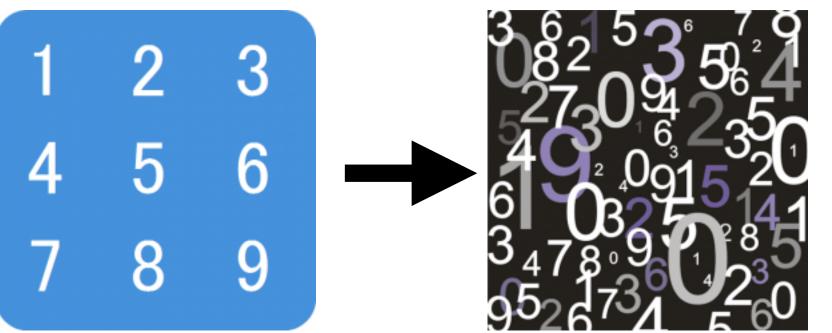




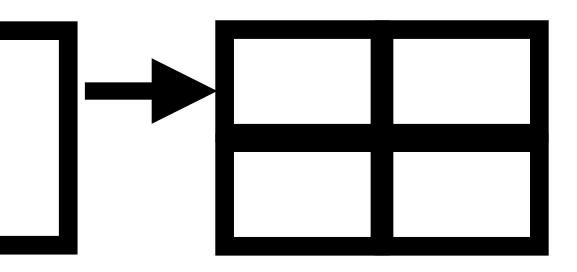
## **Discussion and Defense**

- Generate memory registration keys cryptographically
- Isolate on-board resources for different clients





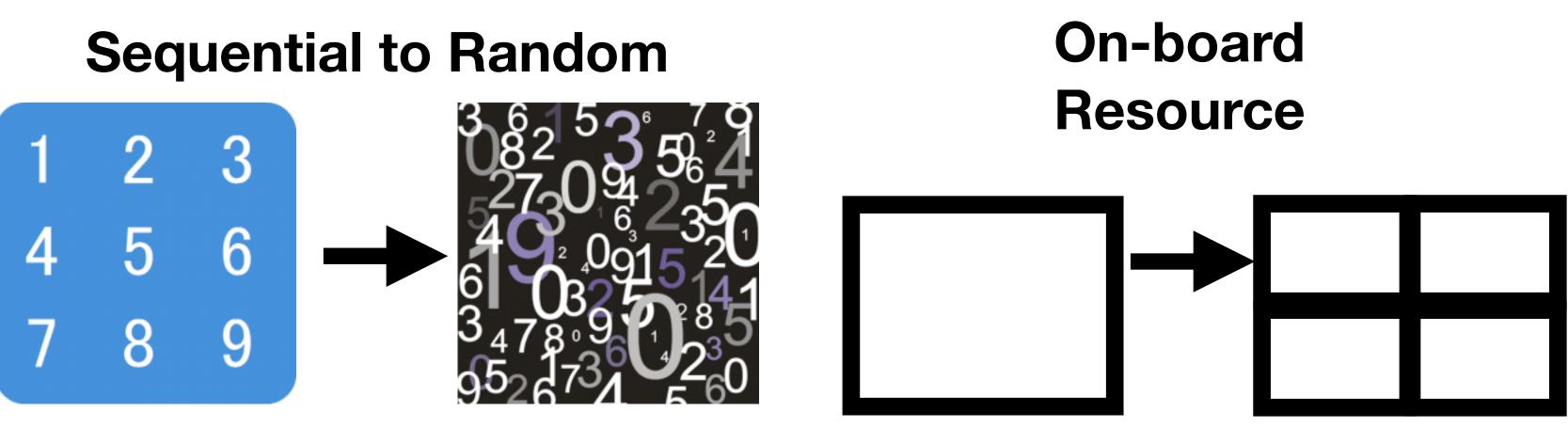
On-board Resource

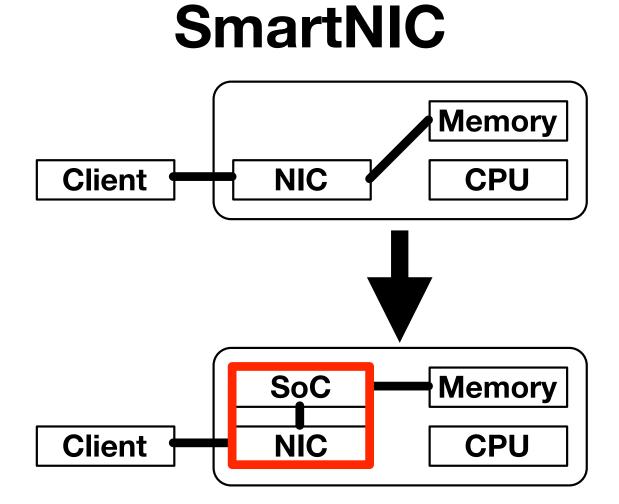




## **Discussion and Defense**

- Generate memory registration keys cryptographically
- Isolate on-board resources for different clients
- Enhancing SmartNIC at the receiver side





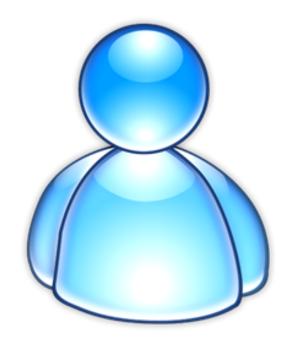


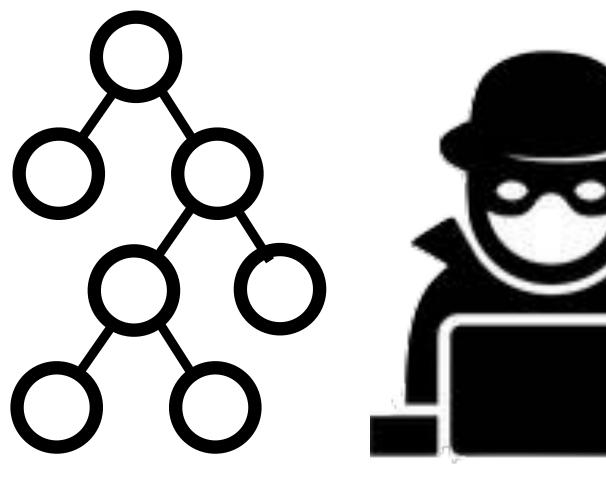


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### **ORAM Access**





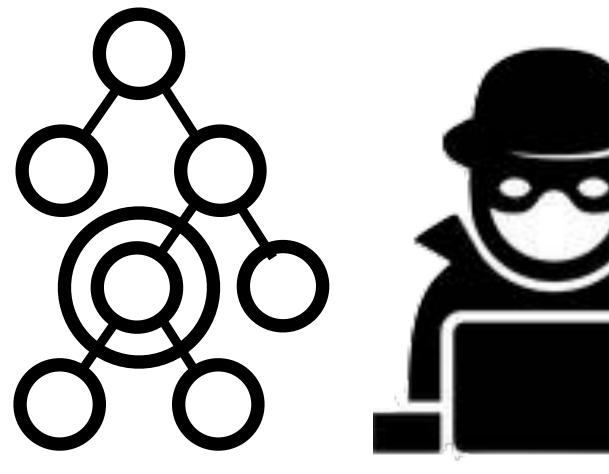




### **ORAM Access**







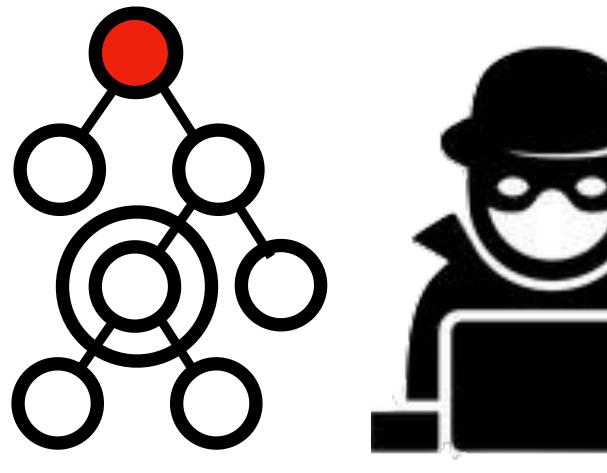




### **ORAM Access**







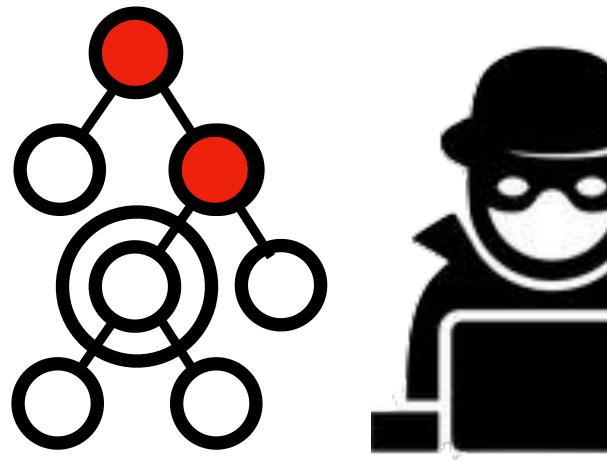




### **ORAM Access**







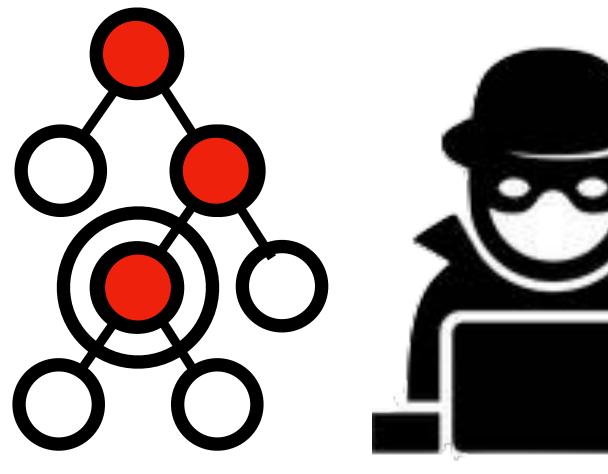




### **ORAM Access**





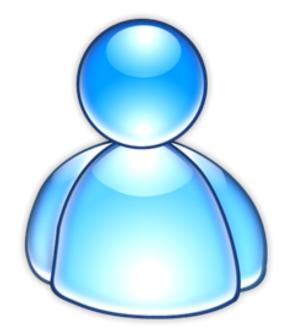


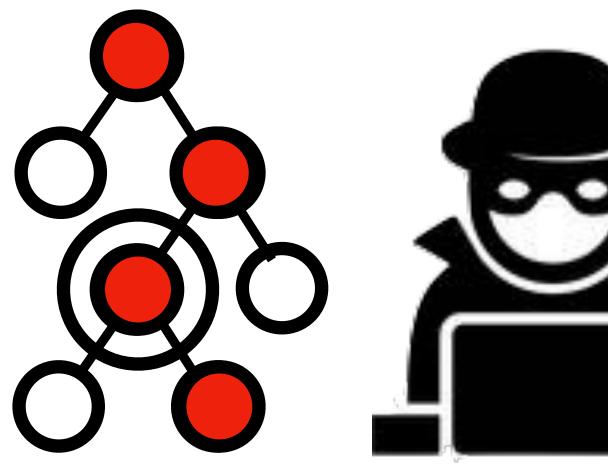




### **ORAM Access**











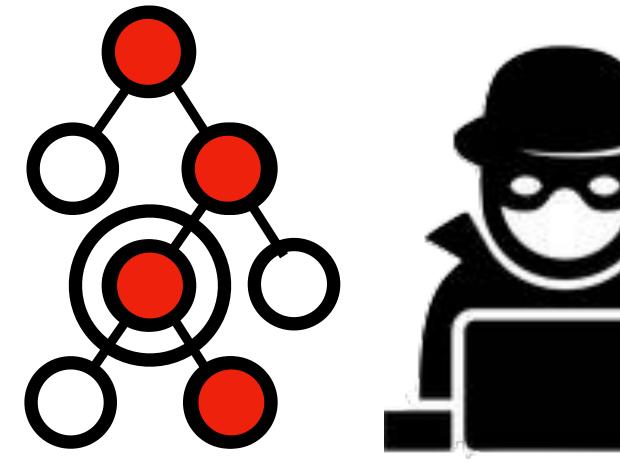
### **ORAM Access**







### **One-sided READ**







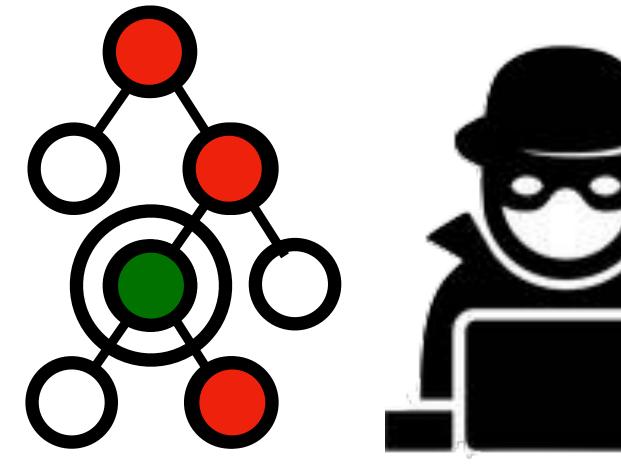
### **ORAM Access**







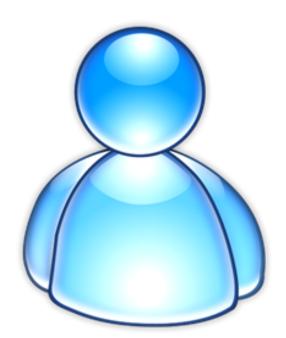
### **One-sided READ**





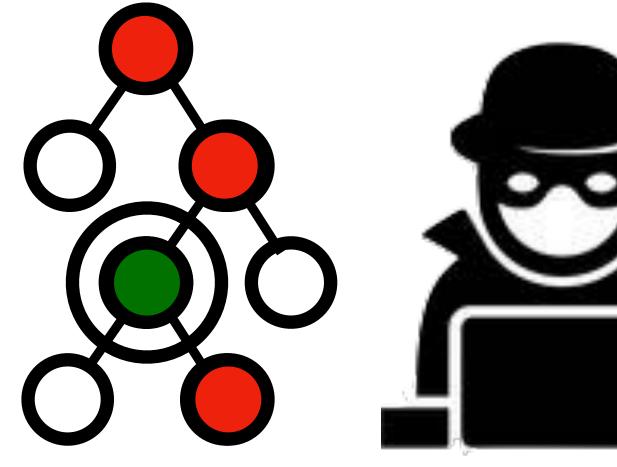


### **ORAM Access** (1-K)% ORAM READ **100% ORAM WRITE**



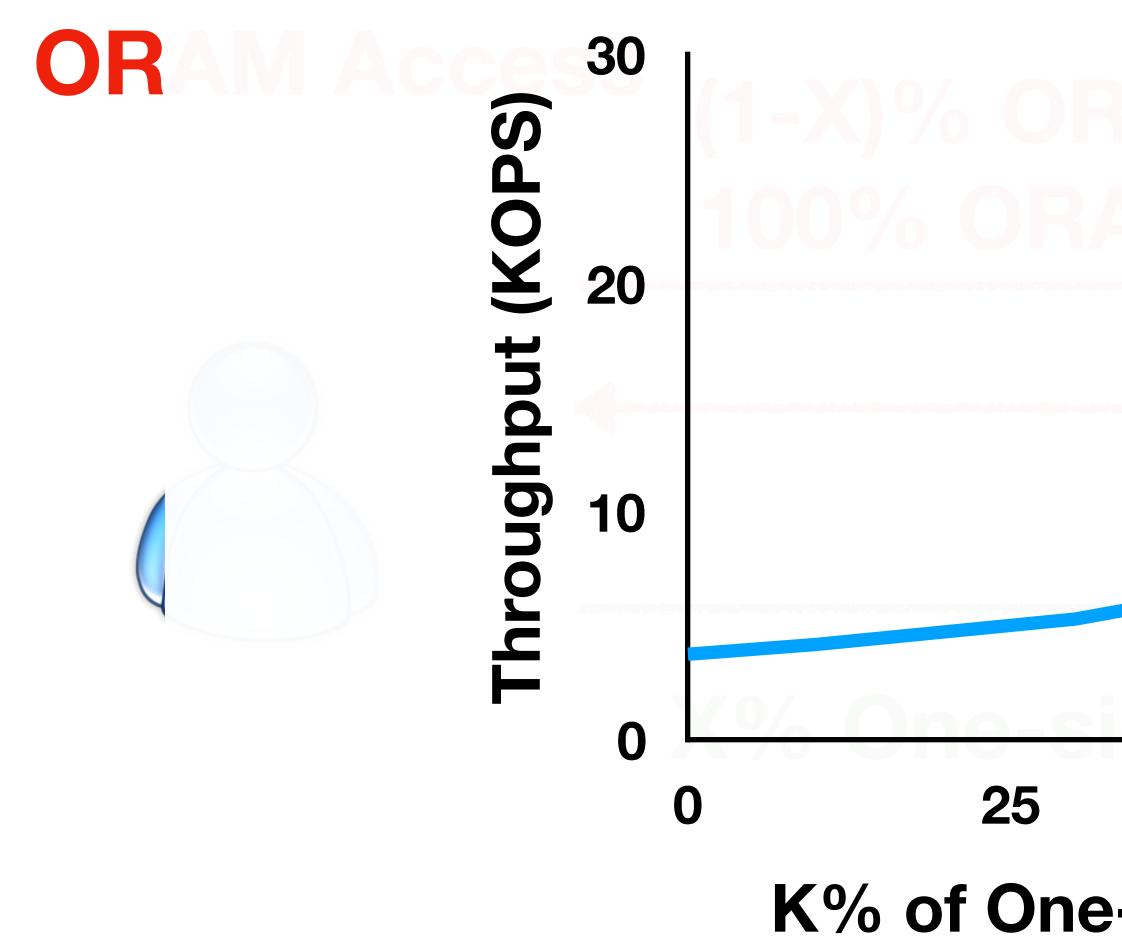












### AM READ M WRITE

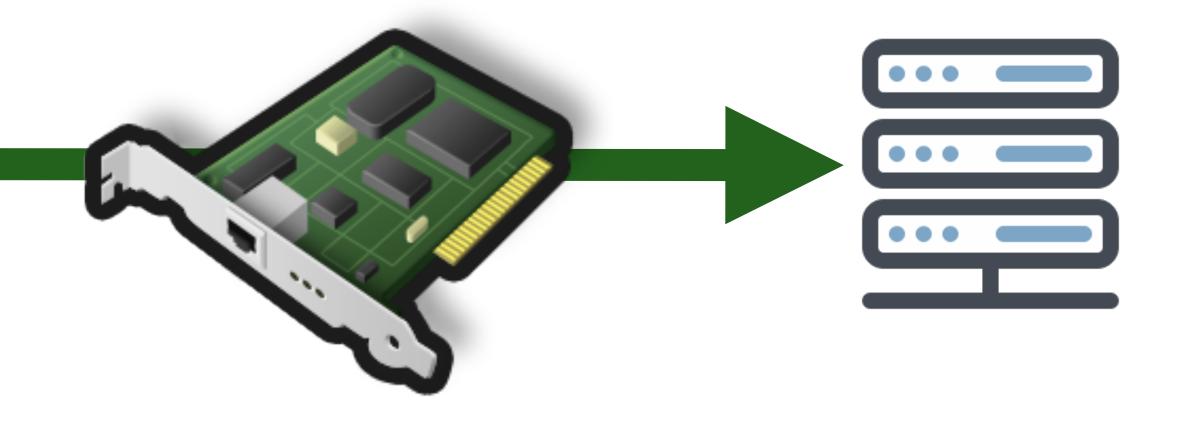
255075100K% of One-Sided READ Operations





- Security concerns of one-sided communication
- Tradeoffs between Performance and Security
- Hardware Vendor, Software Developers, and Datacenter

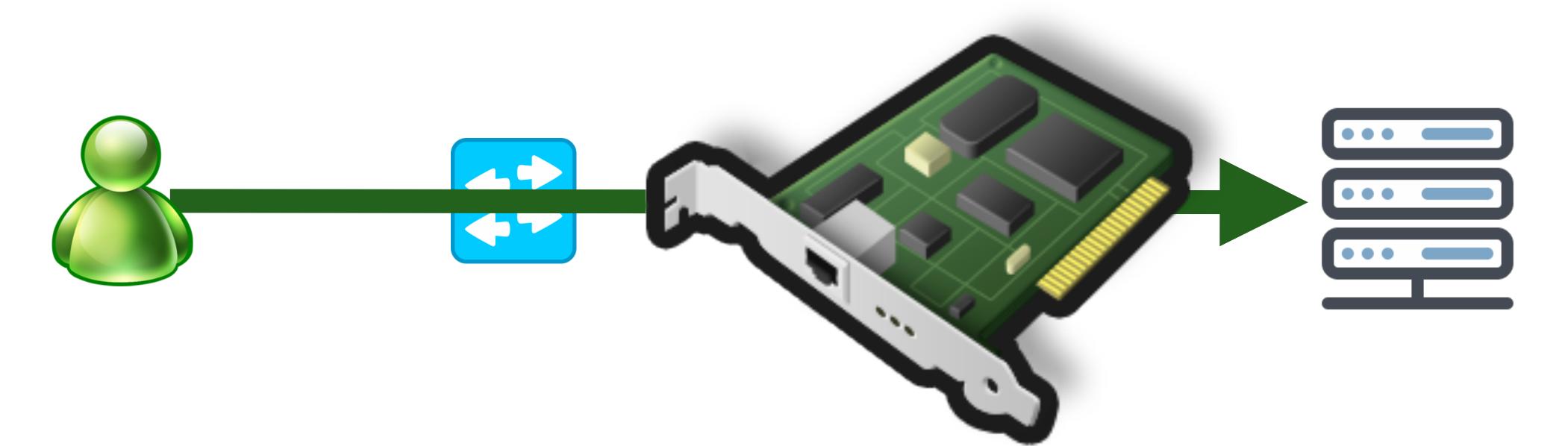








- Security concerns of one-sided communication
- Tradeoffs between Performance and Security
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# Thank you Questions?



