BEN GRAS/@BJG, KAVEH RAZAVI, CRISTIANO GIUFFRIDA, HERBERT BOS VRIJE UNIVERSITEIT AMSTERDAM

## USENIX SECURITY 2018



SPYING ON YOUR NEIGHBOR:
CPU CACHE ATTACKS AND BEYOND

## TEASER

- We would like to protect against cache attacks generically
- You won't believe this one thing that people forget


## OVERVIEW

- Side channels
- Cache attacks
- TLBleed
- Evaluation


## CACHE SIDE CHANNELS



## SIDE CHANNELS

## SIDE CHANNELS

- Leak secrets outside the regular interface


## SIDE CHANNELS

- Leak secrets outside the regular interface



## SIDE CHANNELS

- Leak secrets outside the regular interface

- The first combination safes in the 1950 s


## EXAMPLE: FLUSH+RELOAD

- Can attack AES implementation with T tables
- A table lookup happens $T_{j}\left[x_{i}=p_{i} \oplus k_{i}\right]$
- $p_{i}$ is a plaintext byte, $k_{i}$ a key byte
- We can detect lookups into the table using F+R


## EXAMPLE: FLUSH+RELOAD

- Again: secrets are betrayed by memory accesses
- Known plaintext + accesses = key recovery


## EXAMPLE: FLUSH+RELOAD

- Again: secrets are betrayed by memory accesses
- Known plaintext + accesses = key recovery



## EXAMPLE: LIBGCRYPT ECC

- Not side channel proof version:


## EXAMPLE: LIBGCRYPT ECC

- Not side channel proof version:

```
void _gcry_mpi_ec_mul_point (mpi_point_t result,
gcry_mpi_t scalar, mpi_point_t point,
    mpi_ec_t ctx)
{
    for (j=nbits-1; j >= 0; j--) {
    _gcry_mpi_ec_dup_point (result, result, ctx);
    if (mpi_test_bit (scalar, j))
    _gcry_mpi_ec_add_points(result,result,point,ctx);
}
}
```


## EXAMPLE: LIBGCRYPT ECC

- Not side channel proof version:

EXAMPLE: LIBGCRYPT ECC


## EXAMPLE: LIBGCRYPT ECC



## EXAMPLE: LIBGCRYPT ETC

- More side channel proof version


## EXAMPLE: LIBGCRYPT ETC



## DEFENCE EXAMPLE: TSX

## DEFENCE EXAMPLE:TSX

- Intel TSX: Transactional Synchronization Extensions


## DEFENCE EXAMPLE:TSX

- Intel TSX: Transactional Synchronization Extensions
- Intended for hardware transactional memory


## DEFENCE EXAMPLE:TSX

- Intel TSX: Transactional Synchronization Extensions
- Intended for hardware transactional memory
- But relies on unshared cache activity


## DEFENCE EXAMPLE:TSX

- Intel TSX: Transactional Synchronization Extensions
- Intended for hardware transactional memory
- But relies on unshared cache activity
- Transactions fit in cache, otherwise auto-abort


## DEFENCE EXAMPLE:TSX

- Intel TSX: Transactional Synchronization Extensions
- Intended for hardware transactional memory
- But relies on unshared cache activity
- Transactions fit in cache, otherwise auto-abort
- We can use this as a defence - all solved now right?


## DEFENCE EXAMPLE:TSX

- Intel TSX: Transactional Synchronization Extensions
- Intended for hardware transactional memory
- But relies on unshared cache activity
- Transactions fit in cache, otherwise auto-abort
- We can use this as a defence - all solved now right?



## DEFENCE EXAMPLE:TSX

- Intel TSX: Transactional Synchronization Extensions
- Intended for hardware transactional memory
- But relies on unshared cache activity
- Transactions fit in cache, otherwise auto-abort
- We can use this as a defence - all solved now right?



TLBLEED: TLB AS SHARED STATE

## TLBLEED: TLB AS SHARED STATE

- Other structures than cache shared between threads?
- What about the TLB?
- Documented: TLB has L1iTLB, L1dTLB, and L2TLB
- Not documented: structure

TLBLEED: TLB AS SHARED STATE

## TLBLEED: TLB AS SHARED STATE

- Let's experiment with performance counters
- Try linear structure first
- All combinations of ways (set size) and sets (stride)
- Smallest number of ways is it
- Smallest corresponding stride is number of sets


## TLBLEED: TLB AS SHARED STATE

- Let's experiment with performance counters
- Try linear structure first
- All combinations of ways (set size) and sets (stride)
- Smallest number of ways is it
- Smallest corresponding stride is number of sets



## TLBLEED: TLB AS SHARED STATE

- Let's experiment with performance counters
- Try linear structure first
- All combinations of ways (set size) and sets (stride)
- Smallest number of ways is it
- Smallest corresponding stride is number of sets


TLBLEED: TLB AS SHARED STATE

## TLBLEED: TLB AS SHARED STATE

- For L2TLB:

We reverse engineered a more complex hash function

## TLBLEED: TLB AS SHARED STATE

- For L2TLB:

We reverse engineered a more complex hash function

- Skylake XORs 14 bits, Broadwell XORs 16 bits


## TLBLEED: TLB AS SHARED STATE

- For L2TLB:

We reverse engineered a more complex hash function

- Skylake XORs 14 bits, Broadwell XORs 16 bits
- Represented by this matrix, using modulo 2 arithmetic


## TLBLEED: TLB AS SHARED STATE

- For L2TLB:

We reverse engineered a more complex hash function

- Skylake XORs 14 bits, Broadwell XORs 16 bits
- Represented by this matrix, using modulo 2 arithmetic

$$
H=\left[\begin{array}{llllllllllllll}
1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1
\end{array}\right]
$$

TLBLEED: TLB AS SHARED STATE

## TLBLEED: TLB AS SHARED STATE

- Let's experiment with performance counters


## TLBLEED: TLB AS SHARED STATE <br> - Let's experiment with performance counters

- Now we know the structure.. Are TLB's shared between hyperthreads?


## TLBLEED: TLB AS SHARED STATE

- Let's experiment with performance counters
- Now we know the structure..

Are TLB's shared between hyperthreads?

- Let's experiment with misses when accessing the same set


## TLBLEED: TLB AS SHARED STATE

- Let's experiment with performance counters
- Now we know the structure.. Are TLB's shared between hyperthreads?
- Let's experiment with misses when accessing the same set



## TLBLEED: TLB AS SHARED STATE

- Let's experiment with performance counters
- Now we know the structure.. Are TLB's shared between hyperthreads?
- Let's experiment with misses when accessing the same set



## TLBLEED: TLB AS SHARED STATE

- Let's experiment with performance counters
- Now we know the structure.. Are TLB's shared between hyperthreads?
- Let's experiment with misses when accessing the same set



## TLBLEED: TLB AS SHARED STATE

| Name | year | L1 dTLB |  |  |  |  | LI iTLB |  |  |  |  | L2 sTLB |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | set | w | pn | hsh | shr | set | w | pn | hsh | shr | set | w | pn | hsh | shr |
| Sandybridge | 2011 | 16 | 4 | 7.0 | lin | $\checkmark$ | 16 | 4 | 50.0 | lin | $x$ | 128 | 4 | 16.3 | lin | $\checkmark$ |
| Ivybridge | 2012 | 16 | 4 | 7.1 | lin | $\checkmark$ | 16 | 4 | 49.4 | lin | $x$ | 128 | 4 | 18.0 | lin | $\checkmark$ |
| Haswell | 2013 | 16 | 4 | 8.0 | lin | $\checkmark$ | 8 | 8 | 27.4 | lin | $x$ | 128 | 8 | 17.1 | lin | $\checkmark$ |
| HaswellXeon | 2014 | 16 | 4 | 7.9 | lin | $\checkmark$ | 8 | 8 | 28.5 | lin | $x$ | 128 | 8 | 16.8 | lin | $\checkmark$ |
| Skylake | 2015 | 16 | 4 | 9.0 | lin | $\checkmark$ | 8 | 8 | 2.0 | lin | $x$ | 128 | 12 | 212.0 | XOR-7 | $\checkmark$ |
| BroadwellXeon | 2016 | 16 | 4 | 8.0 | lin | $\checkmark$ | 8 | 8 | 18.2 | lin | $x$ | 256 | 6 | 272.4 | XOR-8 | $\checkmark$ |
| Coffeelake | 2017 | 16 | 4 | 9.1 | lin | $\checkmark$ | 8 | 8 | 26.3 | lin | $x$ | 128 | 12 | 230.3 | XOR-7 | $\checkmark$ |

TLBLEED: TLB AS SHARED STATE

## TLBLEED: TLB AS SHARED STATE

Can we use only latency?

- Map many virtual addresses to same physical page


## TLBLEED: TLB AS SHARED STATE

- Can we use only latency?
- Map many virtual addresses to same physical page


TLBLEED: TLB AS SHARED STATE

## TLBLEED: TLB AS SHARED STATE

- Let's observe EdDSA ECC key multiplication

```
void _gcry_mpi_ec_mul_point (mpi_point_t result,
    gcry_mpi_t scalar, mpi_point_t point,
    mpi_ec_t ctx)
{
    for (j=nbits-1; j >= 0; j--) {
    _gcry_mpi_ec_dup_point (result, result, ctx);
    if (mpi_test_bit (scalar, j))
        _gcry_mpi_ec_add_points(result,result,point,ctx);
    }
}
```


## TLBLEED: TLB AS SHARED STATE

- Let's observe EdDSA ECC key multiplication
- Scalar is secret and ADD only happens if there's a 1

```
void _gcry_mpi_ec_mul_point (mpi_point_t result,
    gcry_mpi_t scalar, mpi_point_t point,
    mpi_ec_t ctx)
{
    for (j=nbits-1; j >= 0; j--) {
    _gcry_mpi_ec_dup_point (result, result, ctx);
    if (mpi_test_bit (scalar, j))
        _gcry_mpi_ec_add_points(result,result,point,ctx);
    }
}
```


## TLBLEED: TLB AS SHARED STATE

- Let's observe EdDSA ECC key multiplication
- Scalar is secret and ADD only happens if there's a 1
- Like RSA square-and-multiply

```
void _gcry_mpi_ec_mul_point (mpi_point_t result,
    gcry_mpi_t scalar, mpi_point_t point,
    mpi_ec_t ctx)
{
    for (j=nbits-1; j >= 0; j--) {
    _gcry_mpi_ec_dup_point (result, result, ctx);
    if (mpi_test_bit (scalar, j))
        _gcry_mpi_ec_add_points(result,result,point,ctx);
    }
}
```


## TLBLEED: TLB AS SHARED STATE

- Let's observe EdDSA ECC key multiplication
- Scalar is secret and ADD only happens if there's a 1
- Like RSA square-and-multiply
- But: we can not use code information! Only data..!

```
void _gcry_mpi_ec_mul_point (mpi_point_t result,
    gcry_mpi_t scalar, mpi_point_t point,
    mpi_ec_t ctx)
{
    for (j=nbits-1; j >= 0; j--) {
    _gcry_mpi_ec_dup_point (result, result, ctx);
    if (mpi_test_bit (scalar, j))
        _gcry_mpi_ec_add_points(result,result,point,ctx);
    }
}
```

TLBLEED: TLB AS SHARED STATE

## TLBLEED: TLB AS SHARED STATE

- Let's find the spatial L1 DTLB separation
- There isn't any
- Too much activity in both blue/green cases


## TLBLEED: TLB AS SHARED STATE

- Let's find the spatial L1 DTLB separation
- There isn't any
- Too much activity in both blue/green cases



## TLBLEED: TLB AS SHARED STATE



TLBLEED: TLB AS SHARED STATE

## TLBLEED: TLB AS SHARED STATE

- Monitor a single TLB set and use temporal information


## TLBLEED: TLB AS SHARED STATE

- Monitor a single TLB set and use temporal information
- Use machine learning (SVM classifier) to tell the difference


## TLBLEED: TLB AS SHARED STATE

- Monitor a single TLB set and use temporal information
- Use machine learning (SVM classifier) to tell the difference



## TLBLEED: TLB AS SHARED STATE

- Monitor a single TLB set and use temporal information
- Use machine learning (SVM classifier) to tell the difference



## TLBLEED: TLB AS SHARED STATE

- Monitor a single TLB set and use temporal information
- Use machine learning (SVM classifier) to tell the difference
- Mor
- Use



## TLBLEED: TLB AS SHARED STATE

- Monitor a single TLB set and use temporal information
- Use machine learning (SVM classifier) to tell the difference



EVALUATION

TLBLEED RELIABILITY: ECC

## TLBLEED RELIABILITY: ECC

| Microarchitecture | Trials | Success | Median BF |
| :--- | ---: | ---: | ---: |
| Skylake | 500 | 0.998 | $2^{1.6}$ |
| Broadwell | 500 | 0.982 | $2^{3.0}$ |
| Coffeelake | 500 | 0.998 | $2^{2.6}$ |
| Total | 1500 | 0.993 |  |

## TLBLEED RELIABILITY: ECC

| Microarchitecture | Trials | Success | Median BF |
| :--- | ---: | ---: | ---: |
| Skylake | 500 | 0.998 | $2^{1.6}$ |
| Broadwell | 500 | 0.982 | $2^{3.0}$ |
| Coffeelake | 500 | 0.998 | $2^{2.6}$ |
| Total | 1500 | 0.993 |  |
|  |  |  |  |

- Single trace capture: 1 ms
- Median end-to-end time: 17 s


## TLBLEED RELIABILITY: ECC

| Microarchitecture | Trials | Success | Median BF |
| :--- | ---: | ---: | ---: |
| Skylake | 500 | 0.998 | $2^{1.6}$ |
| Broadwell | 500 | 0.982 | $2^{3.0}$ |
| Coffeclake | 500 | 0.998 | $2^{2.6}$ |
| Total | 1500 | 0.993 |  |

- Single trace capture: 1 ms
- Median end-to-end time: 17 s


## TLBLEED RELIABILITY: ECC

| Microarchitecture | Trials | Success | Median BF |
| :--- | ---: | ---: | ---: |
| Skylake | 500 | 0.998 | $2^{1.6}$ |
| Broadwell | 500 | 0.982 | $2^{3.0}$ |
| Coffeclake | 500 | 0.998 | $2^{2.6}$ |
| Total | 1500 | 0.993 |  |

- Single trace capture: 1 ms
- Median end-to-end time: 17 s

| Microarchitecture | Trials | Success | Median BF |
| :--- | ---: | ---: | ---: |
| Broadwell (CAT) | 500 | 0.960 | $2^{2.6}$ |
| Broadwell | 500 | 0.982 | $2^{3.0}$ |

## TLBLEED RELIABILITY: RSA

- 1024-bit RSA square-and-multiply in libgcrypt
- Old version
- F+R hardened: conditional pointer swap


## TLBLEED RELIABILITY: RSA

- 1024-bit RSA square-and-multiply in libgcrypt
- Old version
- F+R hardened: conditional pointer swap



## RECEPTION

- Intel: dismissed TLBleed
- OpenBSD disabled Intel HT
- Widespread media coverage, logo thanks to TheRegister
- Wikipedia


## RECEPTION

- Intel: dismissed TLBleed
- OpenBSD disabled Intel HT

- Widespread media coverage, logo thanks to TheRegister
- Wikipedia


## RECEPTION

- Intel: dismissed TLBleed
- OpenBSD disabled Intel HT
- Widespread media coverage, logo thanks to TheRegister

- Wikipedia


## RECEPTION

- Intel: dismissed TLBleed
- OpenBSD disabled Intel HT
- Widespread media coverage, logo thanks to TheRegister
- Wikipedia

- Work also by Kaveh Razavi, Cristiano Giuffrida, Herbert Bos
- Some diagrams in these slides were taken from other work: FLUSH+RELOAD, Cloak
- Yuval Yarom, Katrina Falkner, Peter Peßl, Daniel Gruss


CONCLUSION

- Practical, reliable, high resolution side channels exist outside the cache

- Practical, reliable, high resolution side channels exist outside the cache
- They bypass defenses

- Practical, reliable, high resolution side channels exist outside the cache
- They bypass defenses
- @bjg @kavehrazavi

- Practical, reliable, high resolution side channels exist outside the cache
- They bypass defenses
- @bjg @kavehrazavi
- @vu5ec

- Practical, reliable, high resolution side channels exist outside the cache
- They bypass defenses
- @bjg @kavehrazavi
- @vu5ec
- vusec.net/projects/tlbleed/

- Practical, reliable, high resolution side channels exist outside the cache
- They bypass defenses
- @bjg @kavehrazavi
- @vu5ec
- vusec.net/projects/tlbleed/
- Thank you for listening


