

# Spectre Returns! Speculation Attacks Using Return Stack Buffer

Esmaeil Mohammadian,

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# New vulnerabilities in modern

## Spectre Attacks: Exploiting Speculative Execution

Paul Kocher<sup>1</sup>, Jann Horn<sup>2</sup>, Anders Fogh<sup>3</sup>, Daniel Genkin<sup>4</sup>,  
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<sup>1</sup> Independent ([www.paulkocher.com](http://www.paulkocher.com)), <sup>2</sup> Google Project Zero,  
<sup>3</sup> G DATA Advanced Analytics, <sup>4</sup> University of Pennsylvania and University of Maryland,  
<sup>5</sup> Graz University of Technology, <sup>6</sup> Cyberus Technology,  
<sup>7</sup> Rambus, Cryptography Research Division, <sup>8</sup> University of Adelaide and Data61

Spectre  
v1/v2/Meltdown(v3)

Jan 2018

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Meltdown  
Moritz Lipp<sup>1</sup>, Michael Schwarz<sup>1</sup>, Da  
Stefan Mangard<sup>1</sup>, Paul Kocher<sup>3</sup>, Da  
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Spectre  
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Speculative store  
bypass (v4)

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May 2018

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Spectre Attacks: P...

## Spectre Returns! Speculation Attacks using the Return Stack Buffer

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ative Execution

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SpectreRSB(v5?)  
/ ret2spec

July 2018

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## NetSpectre: Read Arbitrary Memory over Network

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Graz University of Technology

Moritz Lipp  
Graz University of Technology

Martin Schwarzl  
Graz University of Technology

Daniel Gruss  
Graz University of Technology

Spectre  
v1/v2/Meltdown(v3)

Spectre v1.1

Spectre v1.2

SGXspectre

Speculative store  
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SpectreNG

SpectreRSB(v5?)  
/ret2spec

NetSpectre

Jan 2018

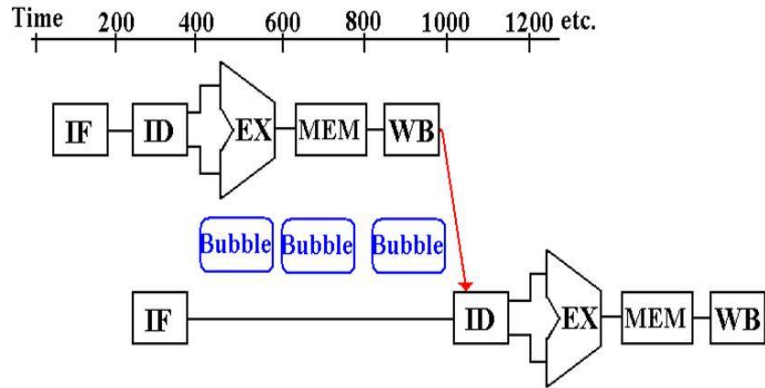
May 2018

July 2018

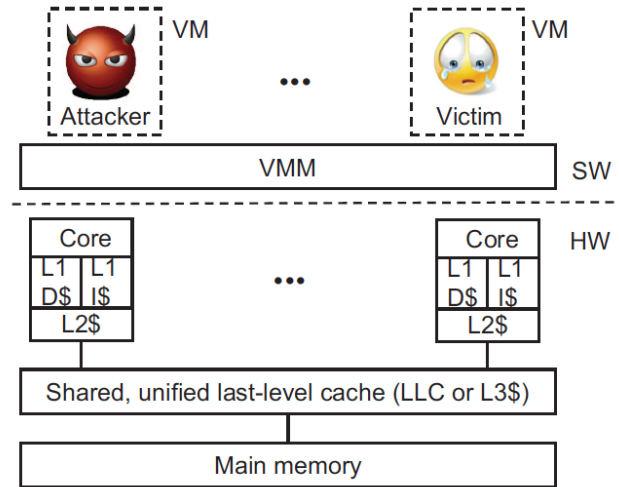
Aug 2018

# Main components of the Attack

## Out of Order Execution

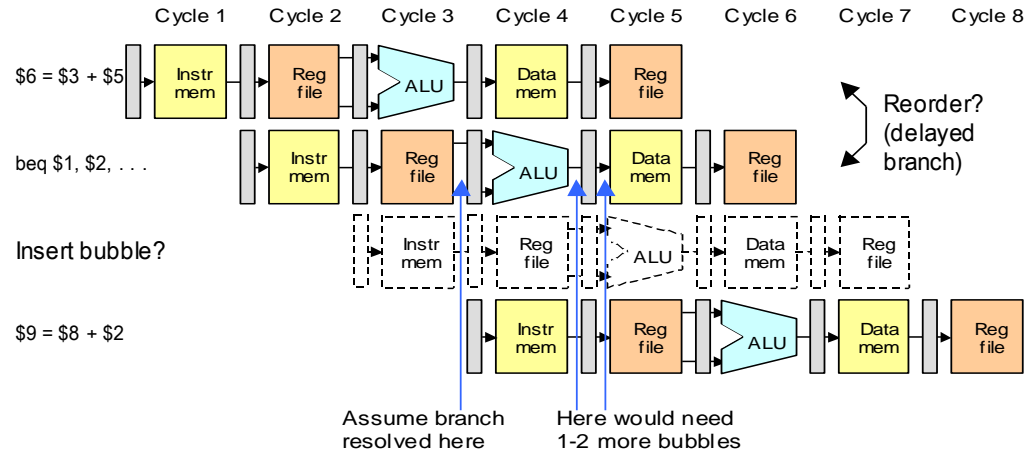


## Side channel Attack



# Out of Order Execution(OoO)

- Speculation is critical to modern CPU performance





# (OoO): Branch predictors

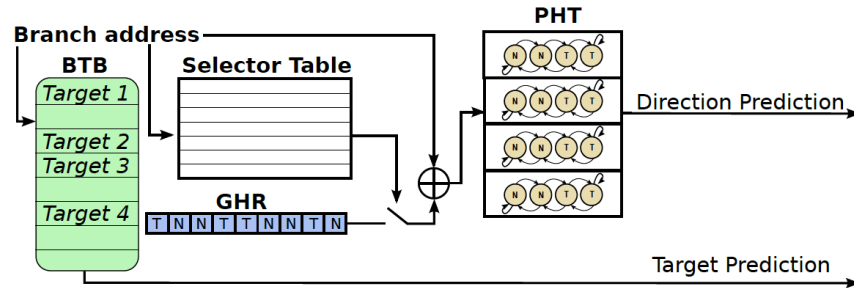
- During speculation processors **guess** the future stream instructions of the program
- Better prediction improve the performance by increasing number of the committed instruction



# Branch predictors

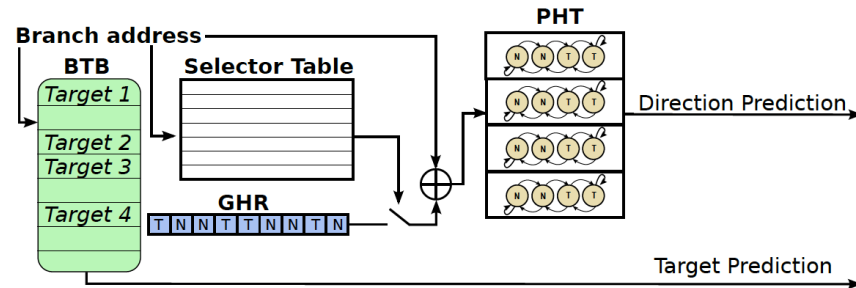
# Branch predictors

- Two hardware predictors:



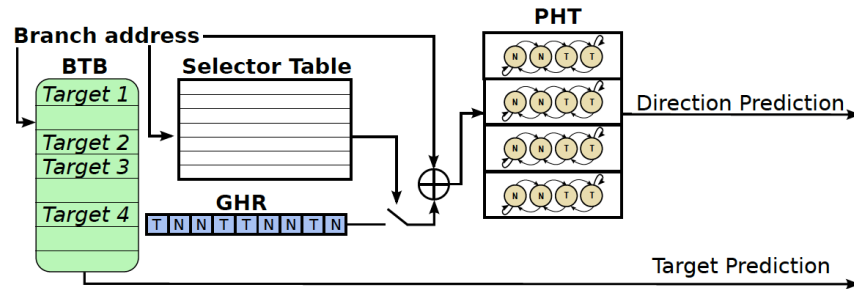
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  - **Direction predictor** guesses if branch is taken or not-taken (PHT)



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- Two hardware predictors:
  - **Direction predictor** guesses if branch is taken or not-taken (PHT)
  - **Target predictor** guesses the target of the branches (BTB)



# Cache Side channel Attacks

- Access to the data inside the cache is fast
- Loading data from memory is too slow

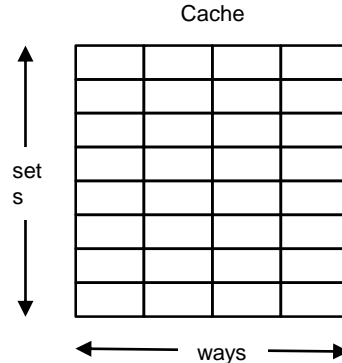
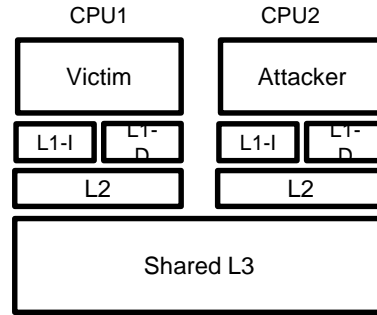


# Cache Side channel Attacks

- Access to the data inside the cache is fast
- Loading data from memory is too slow
- Exploits timing differences that are introduced by the caches
  - Flush and reload
  - Prime and probe
  - ...

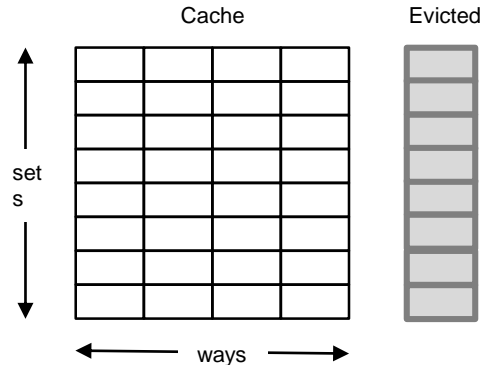
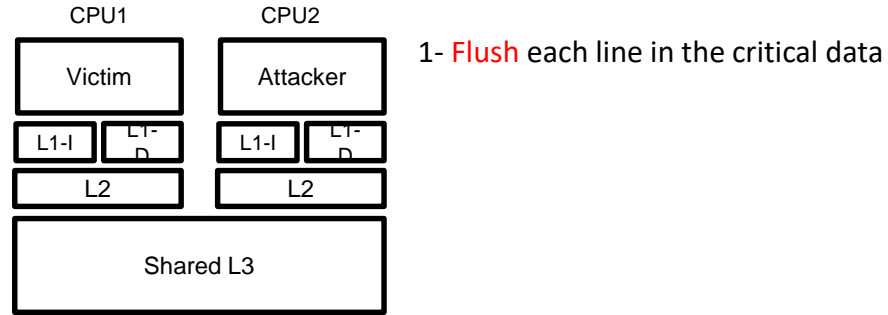


# Side channel: Flush+Reload Attack



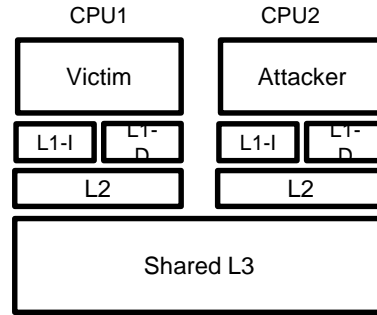


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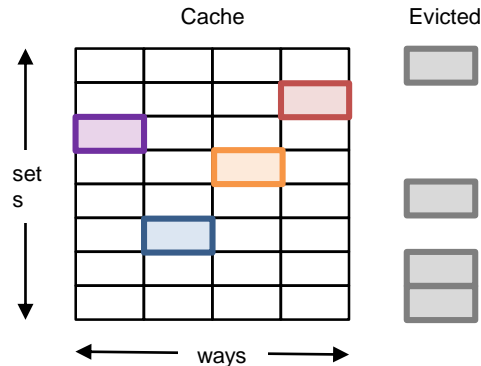


# Side channel: Flush+Reload Attack

2- Victim accesses critical data

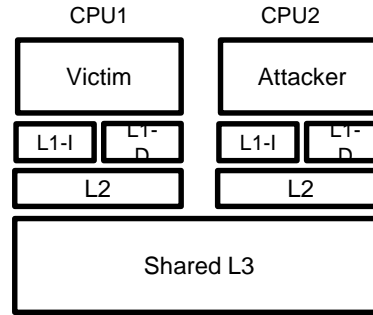


1- Flush each line in the critical data

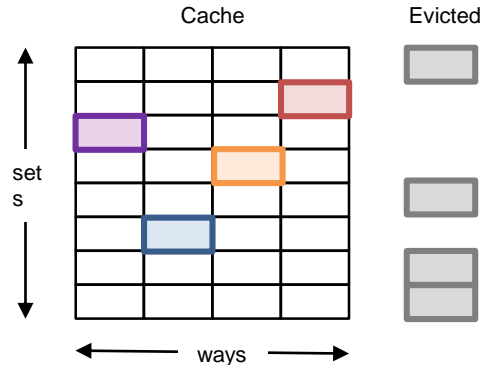


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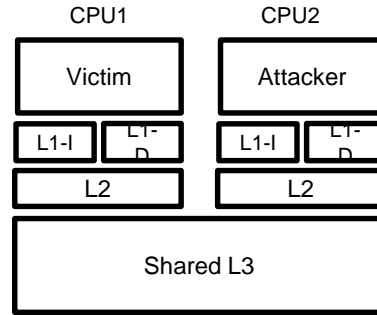


- 1- **Flush** each line in the critical data
- 3- **Reload** critical data (measure time)

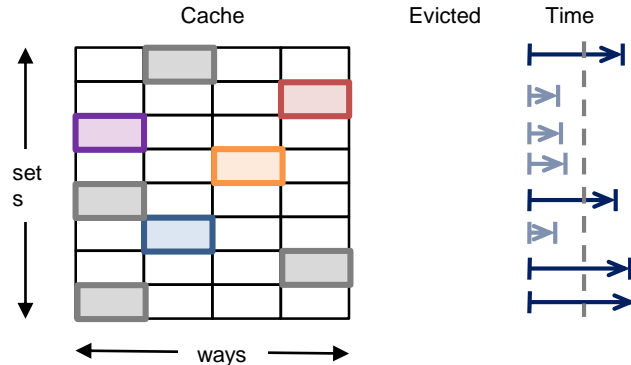


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# Putting it all together– Attacks!



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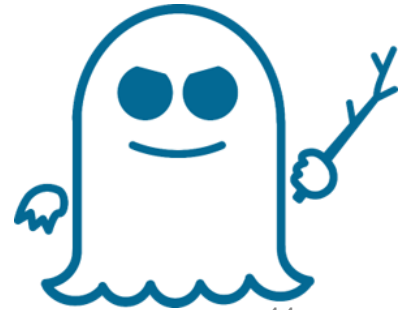


# Main idea of all Attacks

1. Fool the processor to speculatively execute some instructions such that:
  - The instructions access sensitive data without permission (microarchitectural state changes)
  - Load the data into the cache
2. Read it from the side channel → broke isolation
  - Microarchitectural changes are not visible directly

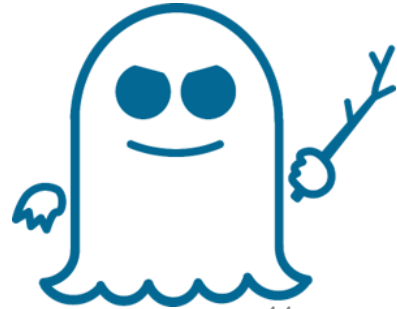


# Example of attacks



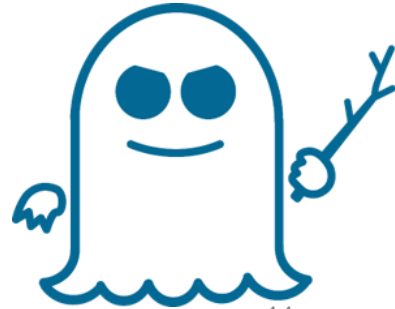
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  - Train the Direction predictor (PHT) to bypass bound checking and leak sensitive data.



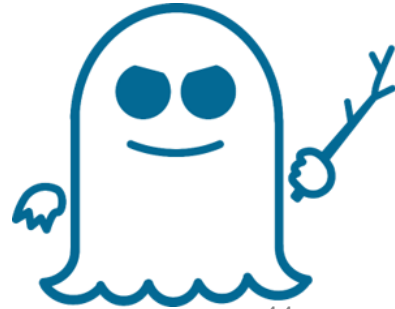
# Example of attacks

- Spectre Variant 1:
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- Spectre Variant 2:



# Example of attacks

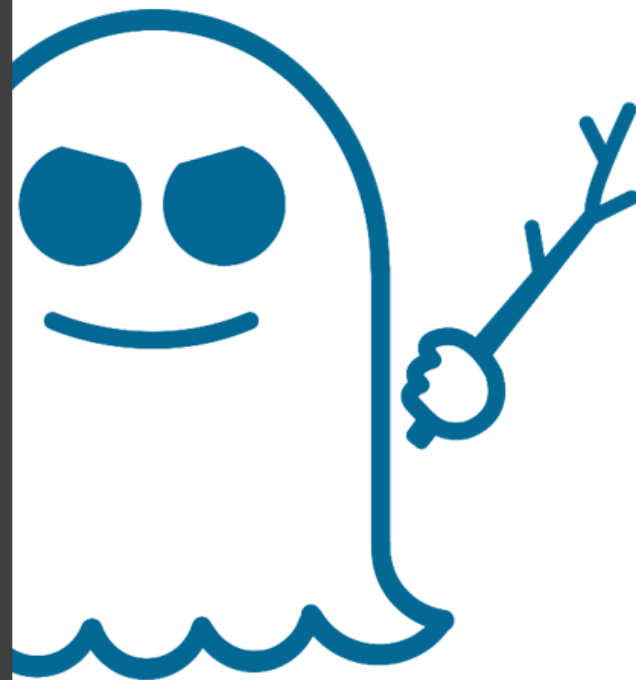
- Spectre Variant 1:
  - Train the Direction predictor (PHT) to bypass bound checking and leak sensitive data.
- Spectre Variant 2:
  - Pollute the target predictor (BTB) by injecting the address of malicious gadget into the BTB
  - Waiting for the victim to execute the malicious gadget speculatively and load sensitive data to the cache



# Spectre returns!

---

Speculation Attacks using  
the Return Stack Buffer



# Why Return Stack Buffer (RSB)?

- BTB can not predict the target of ret instructions properly.

0x0001	printf: ...
0x0005	ret
A:	call printf
0x0010	load
B:	call printf
0x0020	load

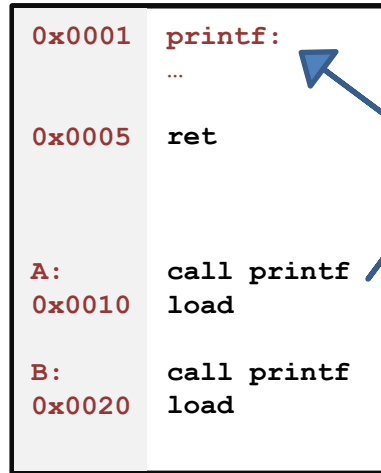
Branch Target Buffer

v	tag	target
1		
1		
0		



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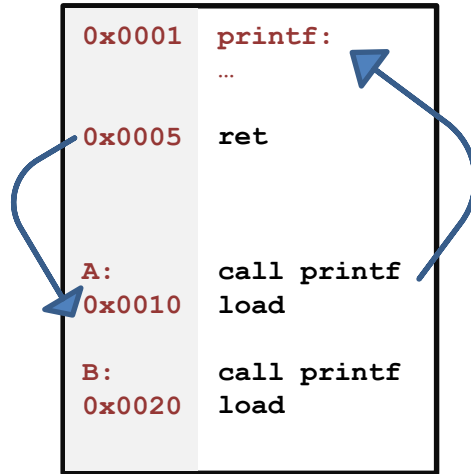


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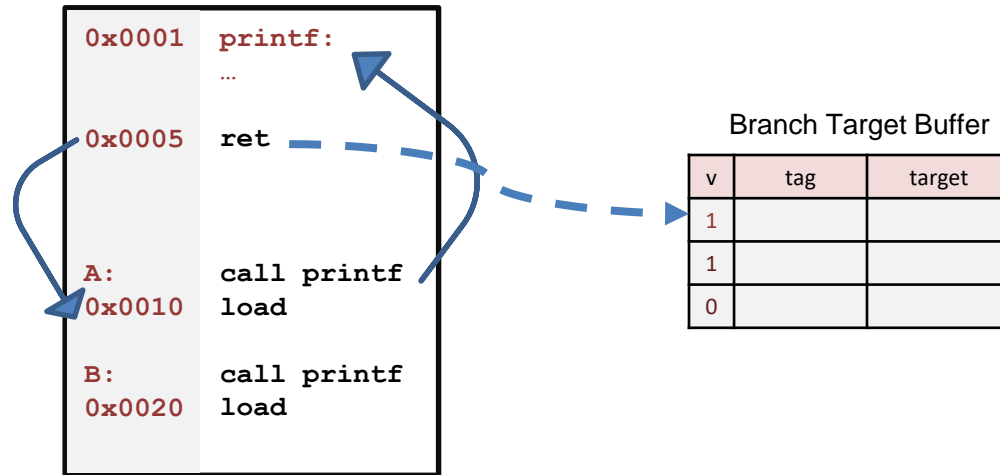


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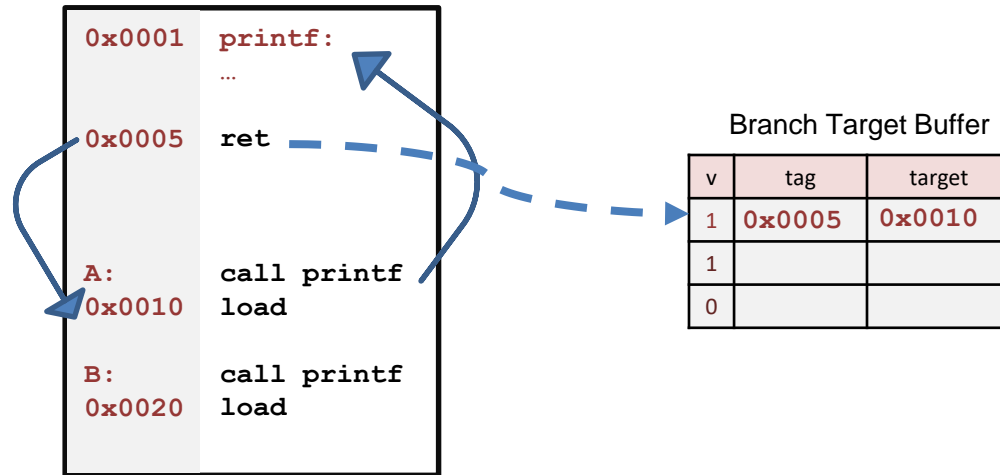
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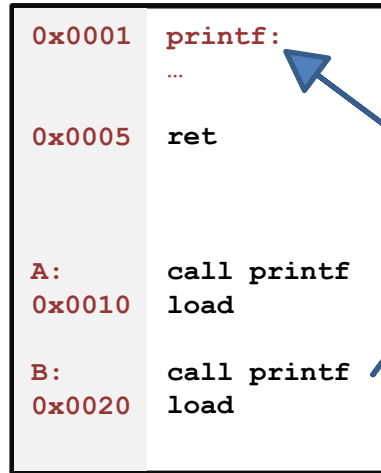
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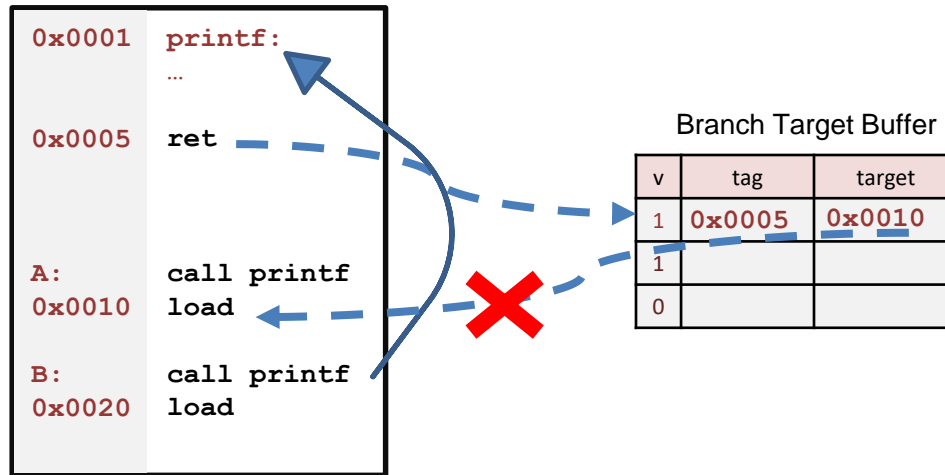


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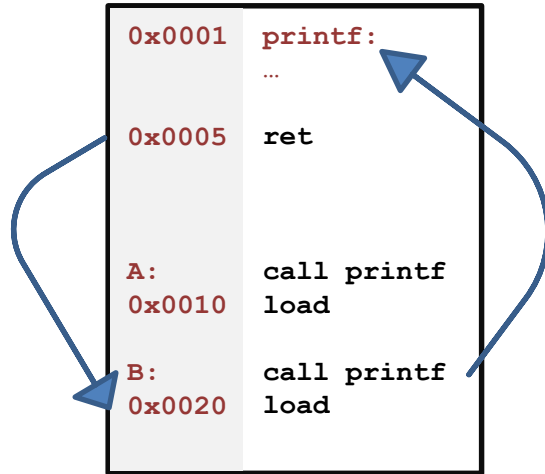
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- Push  $pc+4$  onto the RSB on each *call* instruction
- Pop an address off the RSB on each *ret* instruction

# RSB Pollution

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- Return Stack Buffer works perfectly for matched *call/ret* pairs.



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- Return Stack Buffer works perfectly for matched *call/ret* pairs.
- RSB miss-speculates if return address in the RSB does not match the return address value in the software stack.

# How to pollute RSB?



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S1

Overfill or Underfill of the RSB

S2

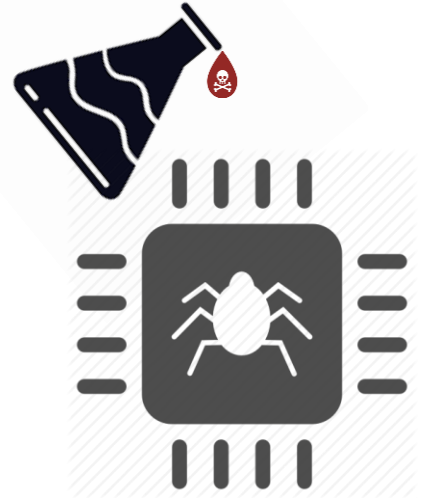
Direct pollution of the RSB

S3

Speculative pollution of the RSB

S4

RSB uses across execution contexts



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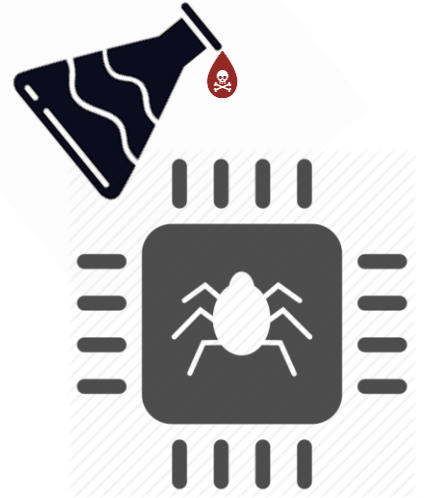
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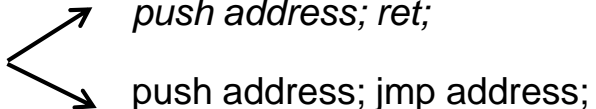
# Direct pollution of the RSB

- `ret` → `pop; jmp address;`
- `call`  `push address; ret;`  
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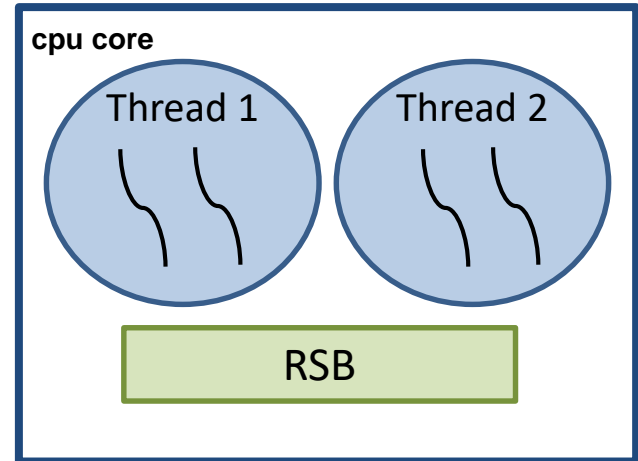
- **ret** → `pop; jmp address;`
  - Leave a value on RSB that has been removed from the software stack
- **call**  `push address; ret;`  
`push address; jmp address;`

# Direct pollution of the RSB

- **ret** → `pop; jmp address;`
  - Leave a value on RSB that has been removed from the software stack
- **call** 
  - A return value exists on the software stack that is not matched by a value in the RSB

# RSB use across execution contexts

- On a context switch the RSB values left over from an executing thread are reused by the next thread





# SpectreRSB

- Attack 1: Same process
- Attack 2: Across threads/process
  - Colluding threads (user)
  - Colluding threads (kernel)
  - Cross-process
- Attack 3: Return in SGX
- Attack 4: Kernel from user

# Attack 1: Basic Attack

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- Lunched from a process to part of its own address space
- Break Sandbox boundaries
  - Difficult to implement the gadget to manipulate the stack using high level sandboxing primitives
- Enables the attacker to read kernel memory via the Meltdown bug
  - KPTI prevents it

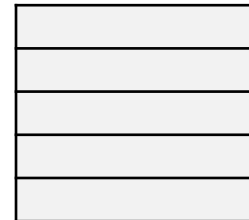
# Attack 1: Basic Attack

```
0x00000010  pollute:  
              push %rbp  
              mov  %rsp,%rbp  
              pop  %rdi  
              pop  %rdi  
              pop  %rdi  
              pop  %rdi  
              pop  %rbp  
              clflush (%rsp)  
0x00000019  retq  
  
0x00000020  speculative:  
0x00000021  call pollute  
0x00000022  movzx (%[array],rbx)   
  
0x00000030  main:  
0x00000031  call speculative  
0x00000032  rdtscp  
              access  
              rdtscp
```

Software Stack

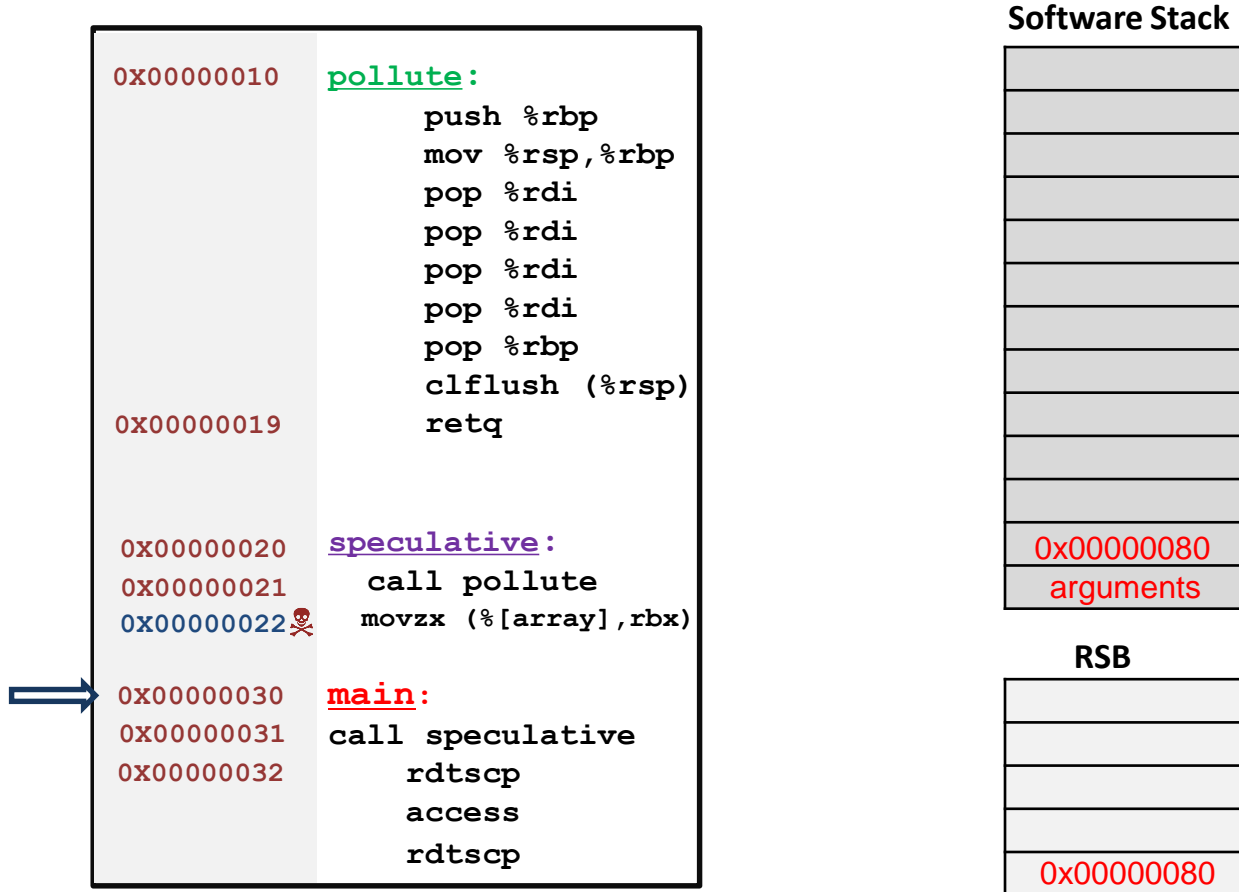


RSB

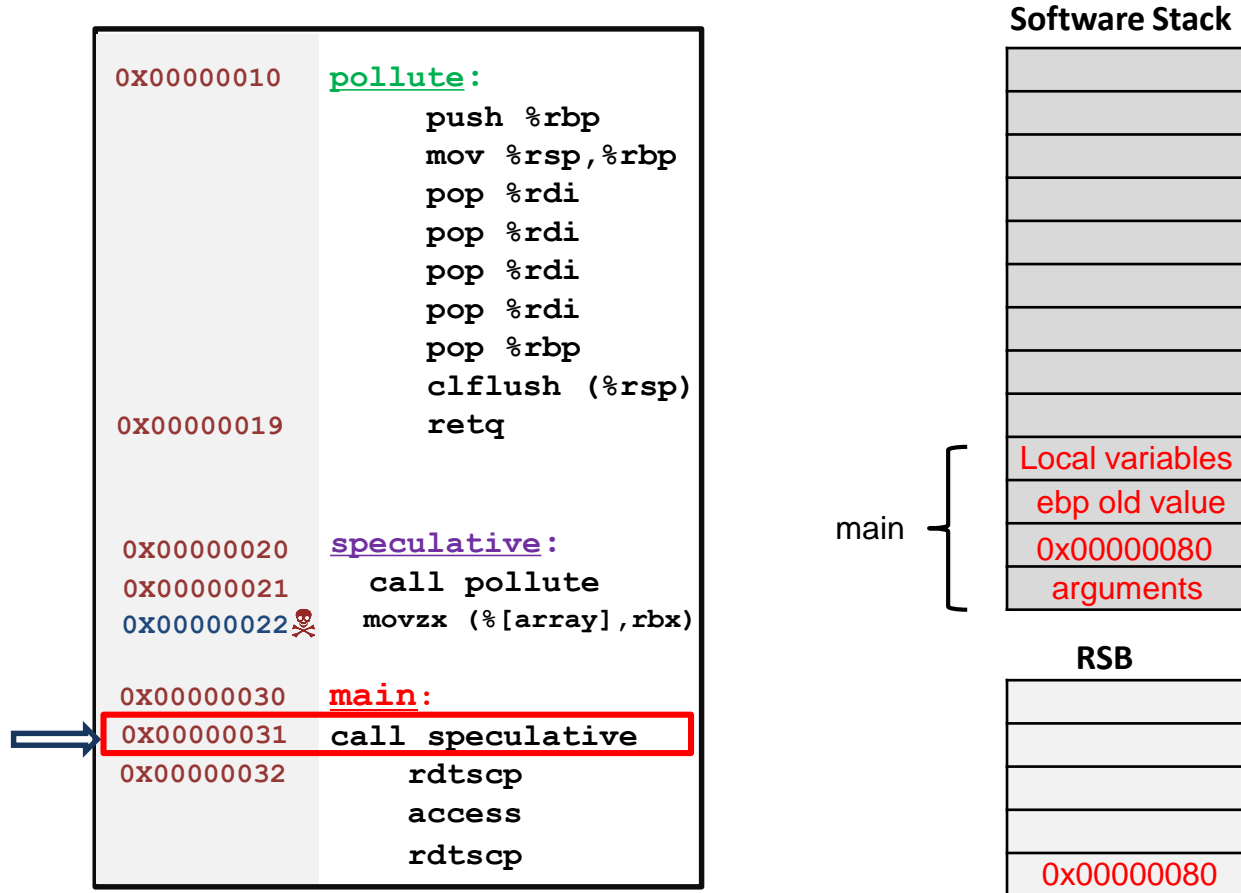




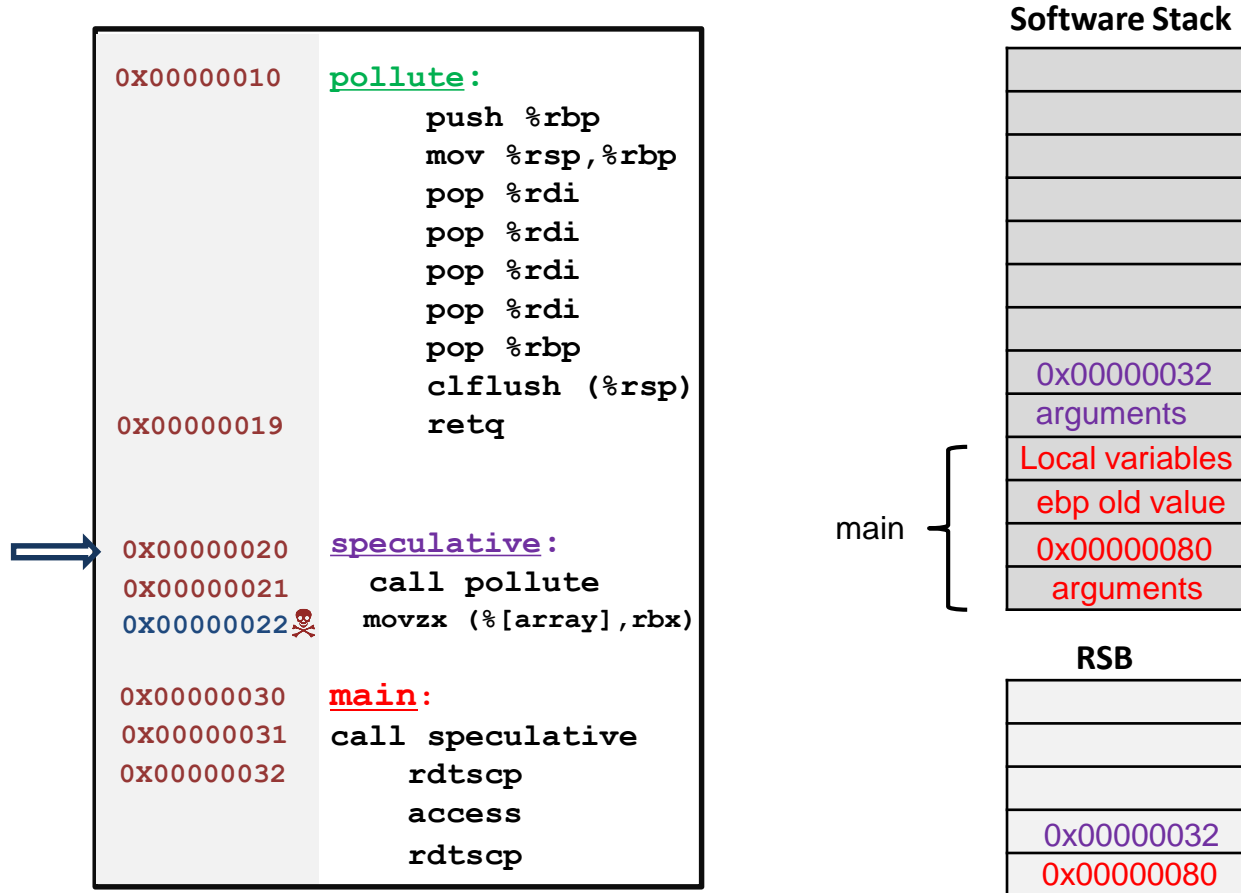
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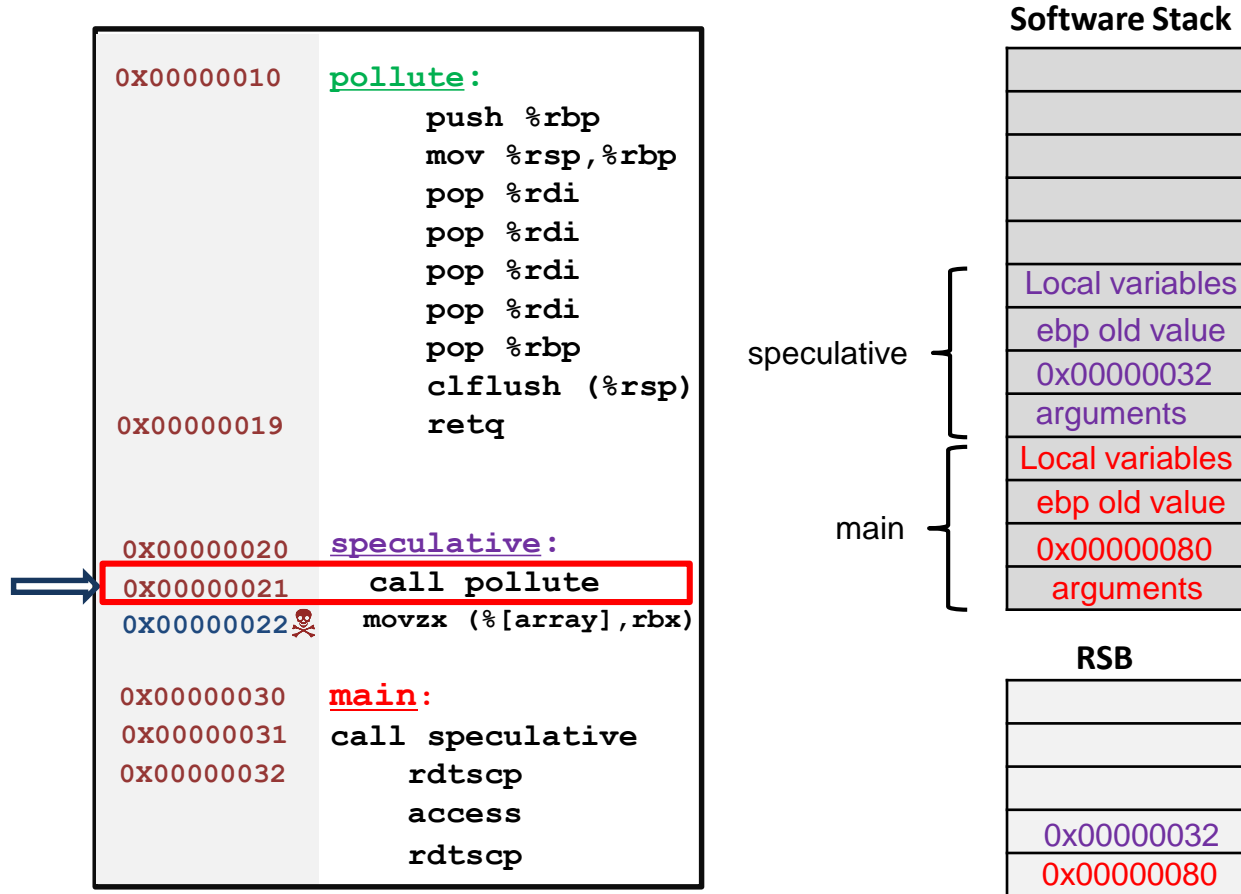
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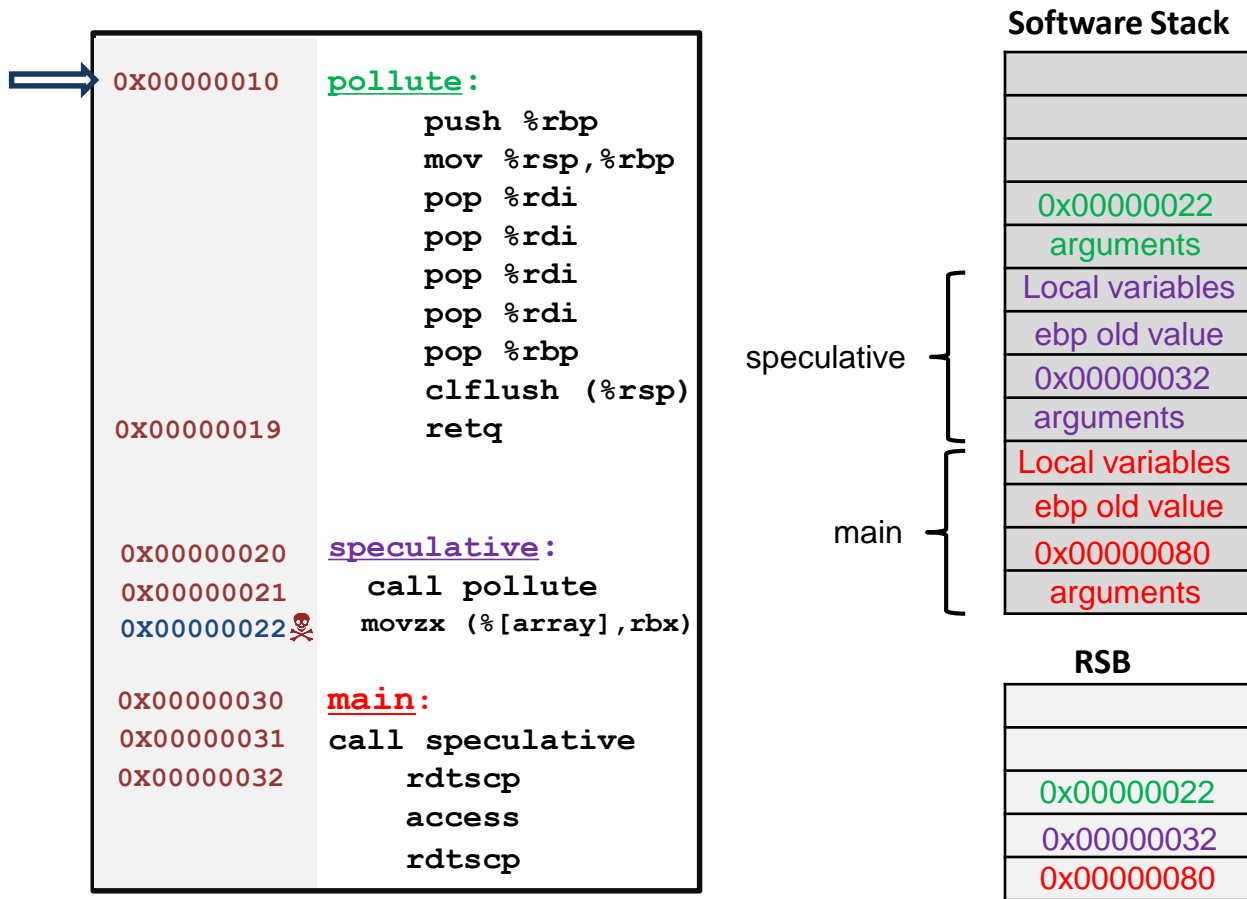
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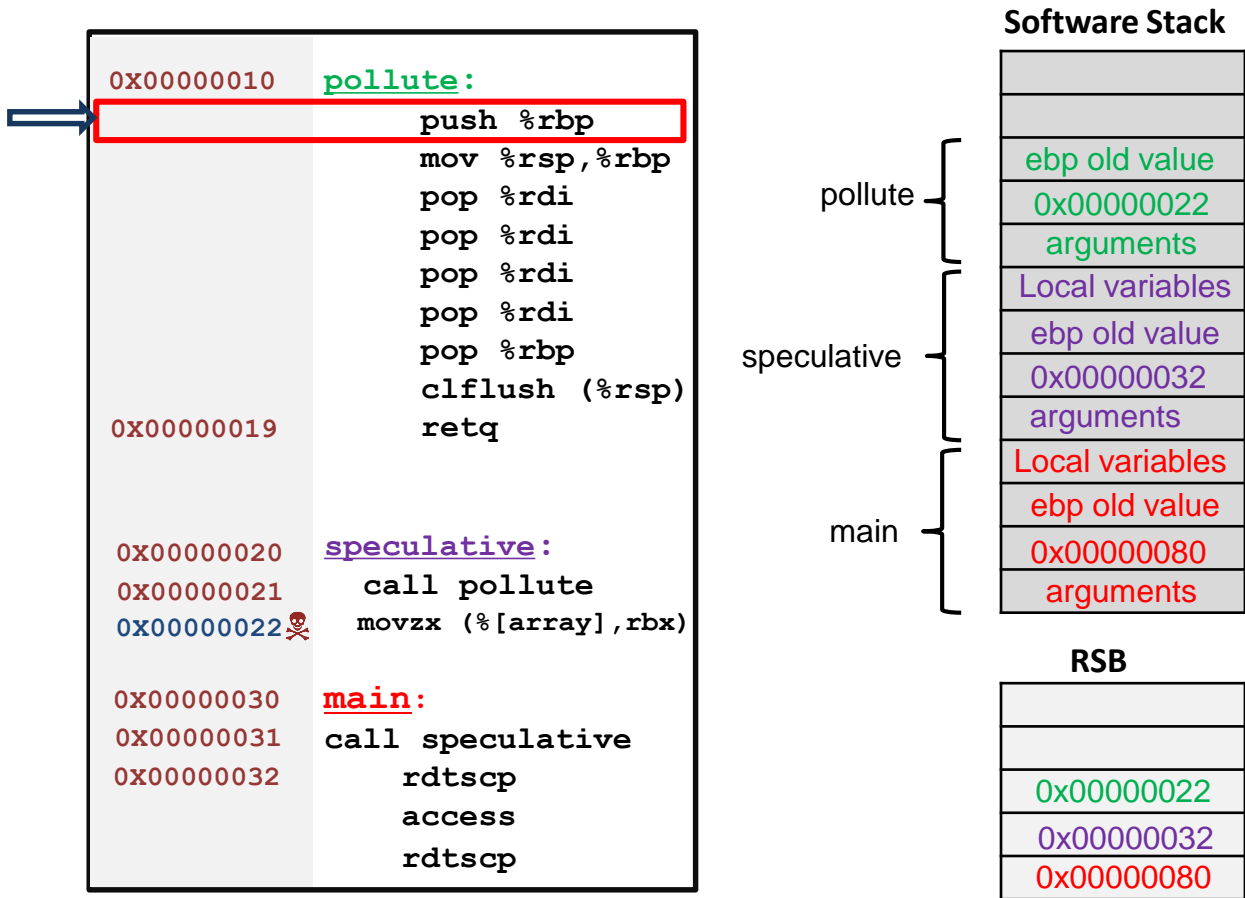
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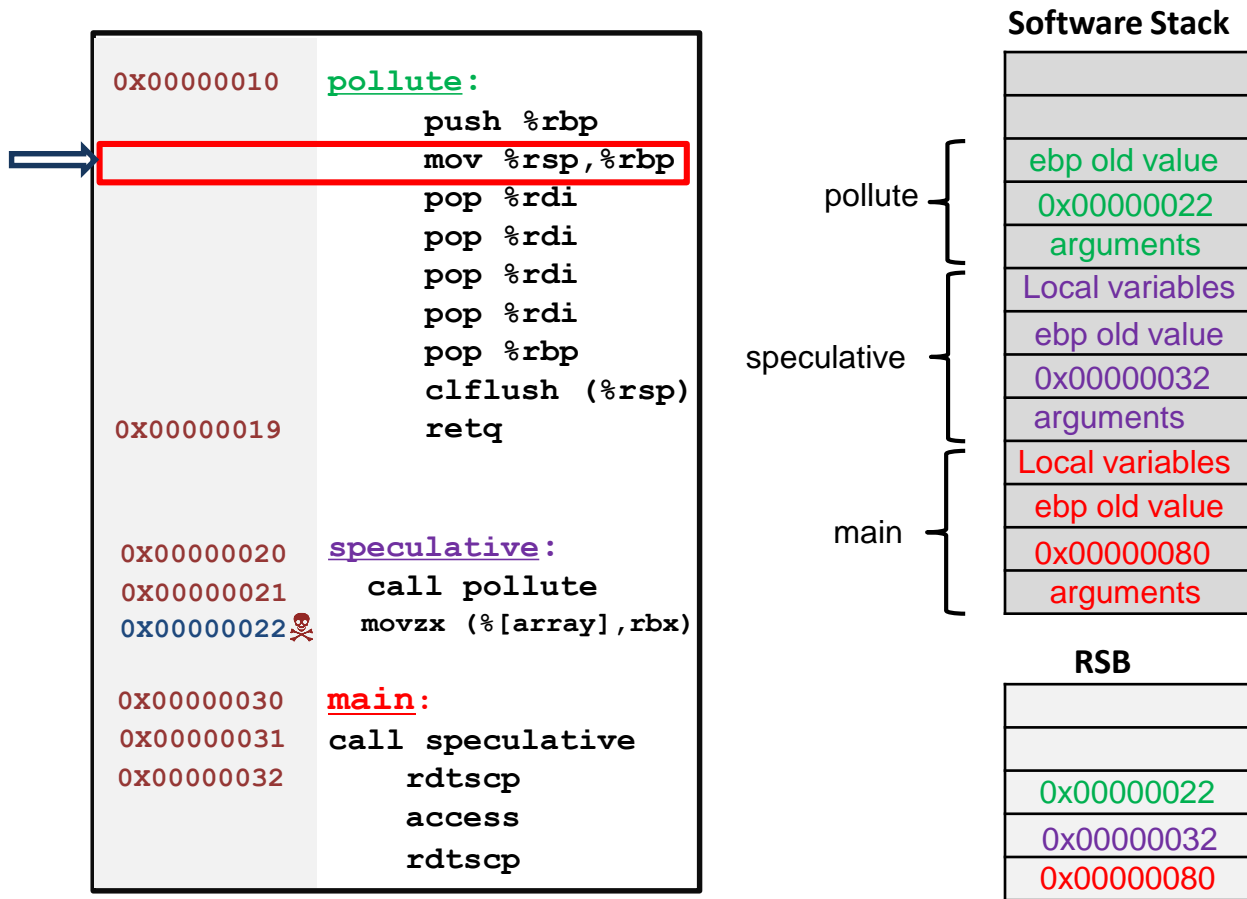
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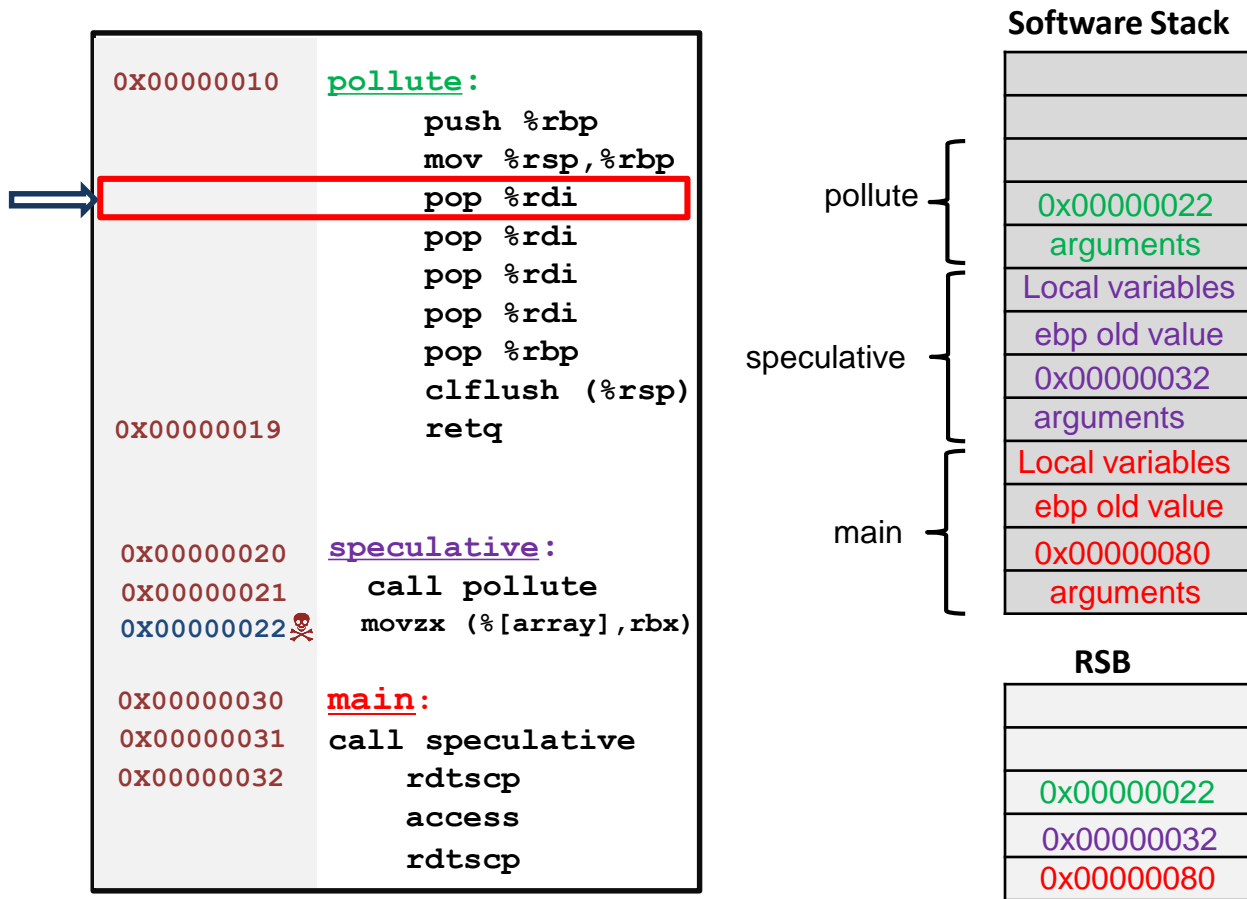
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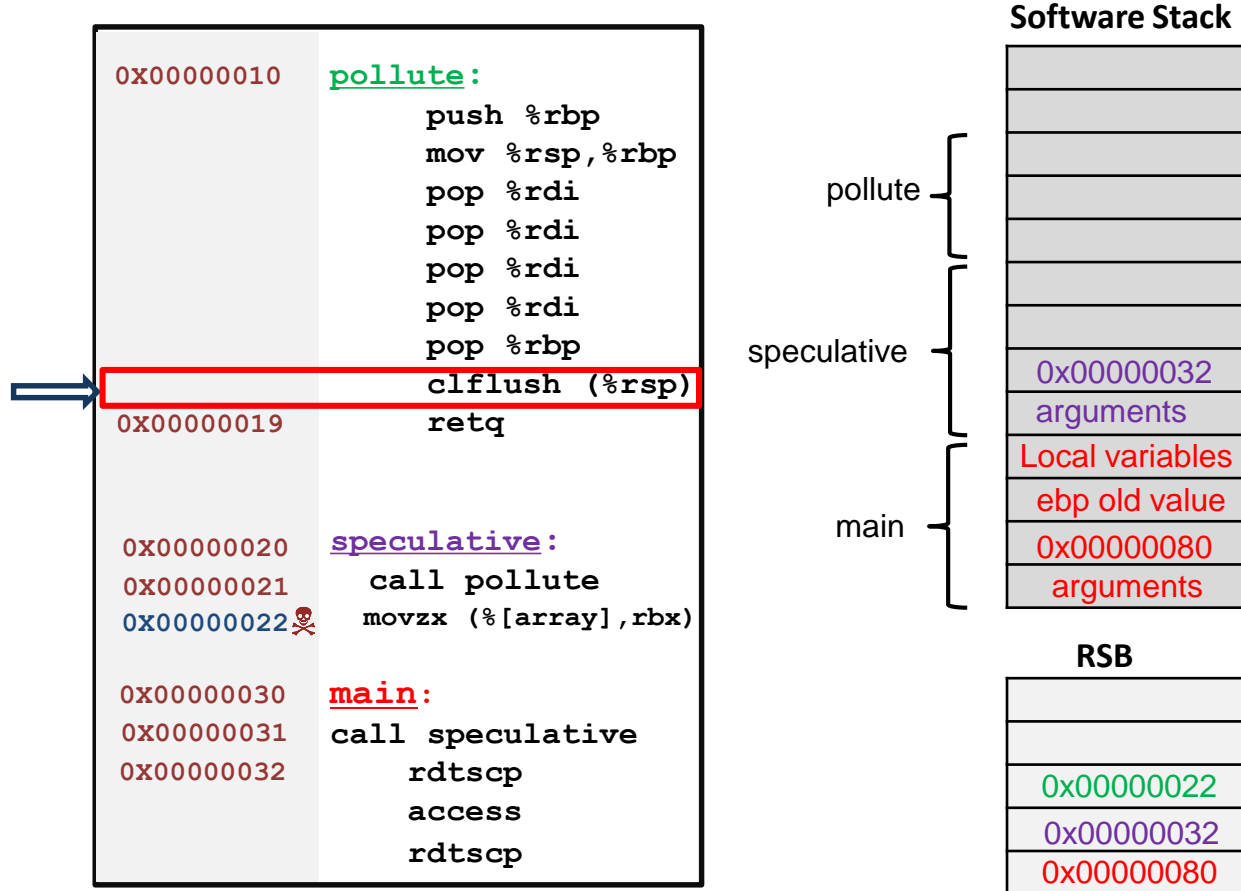


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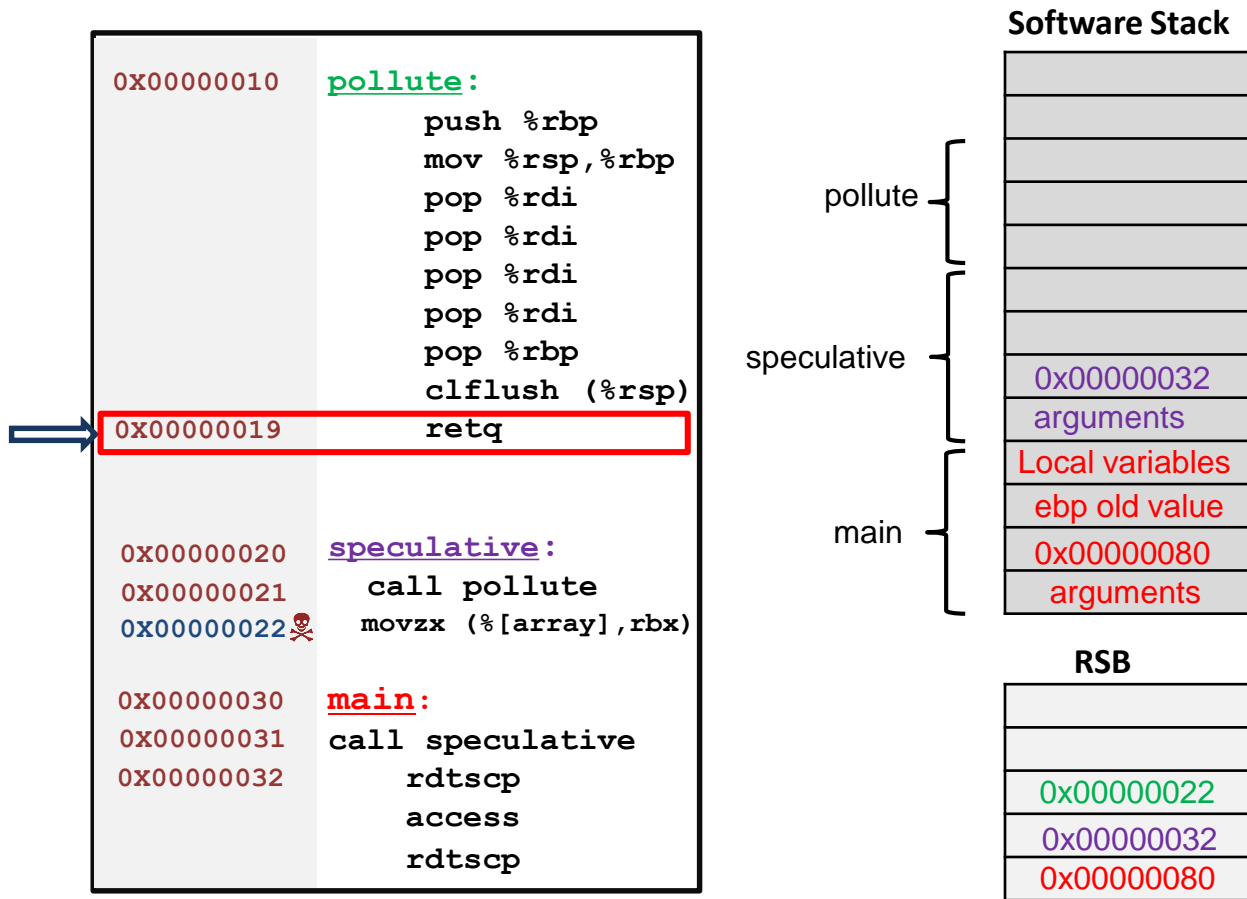




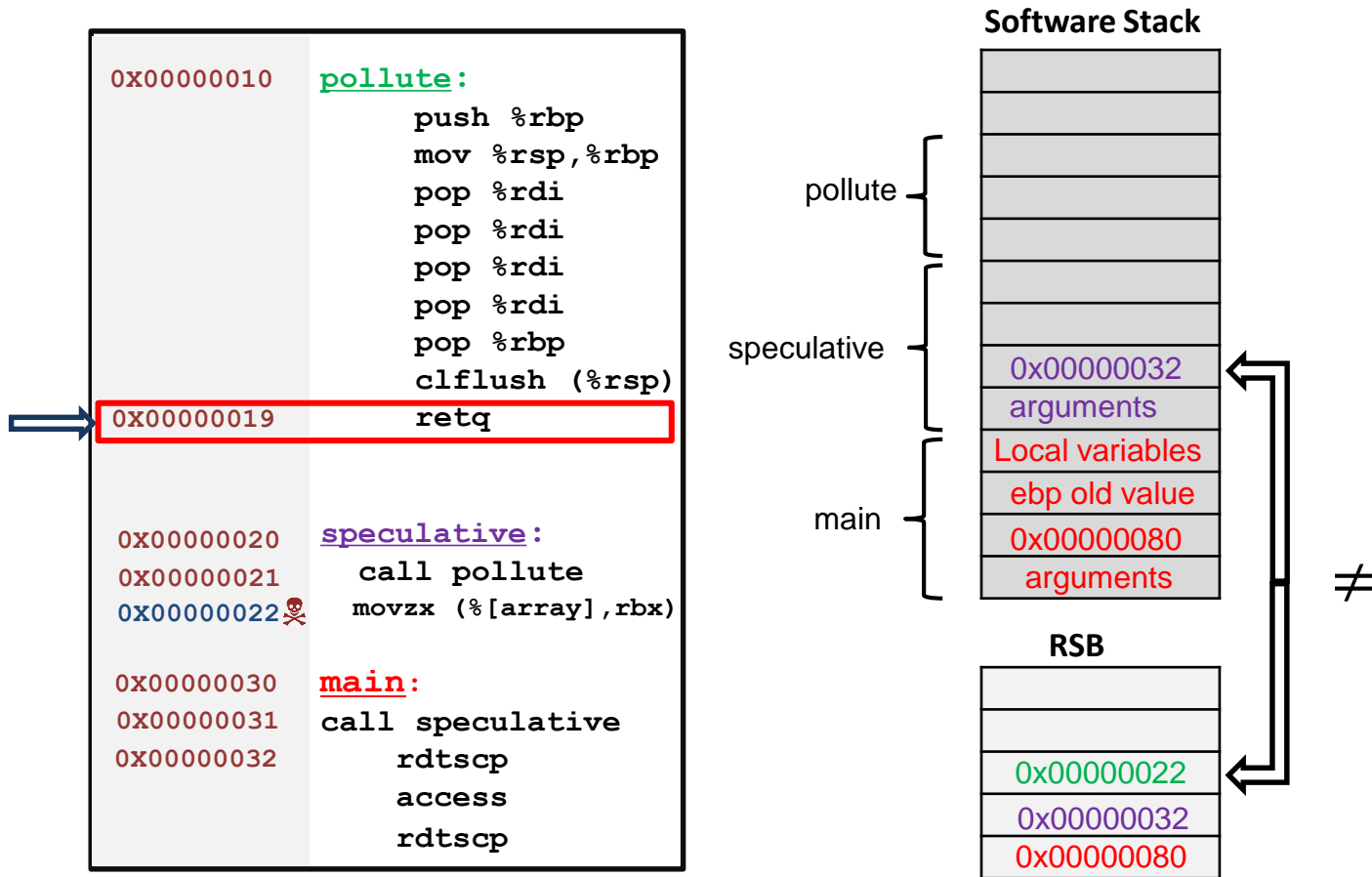
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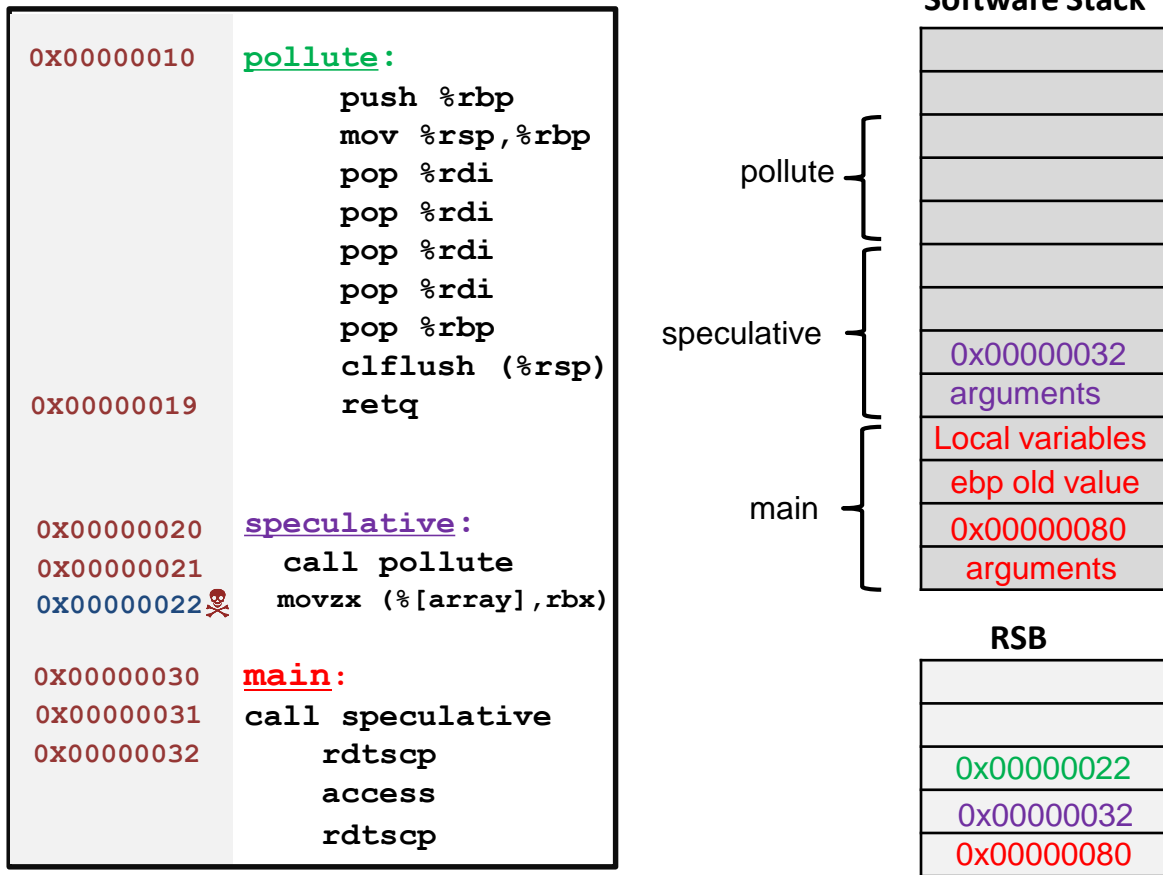
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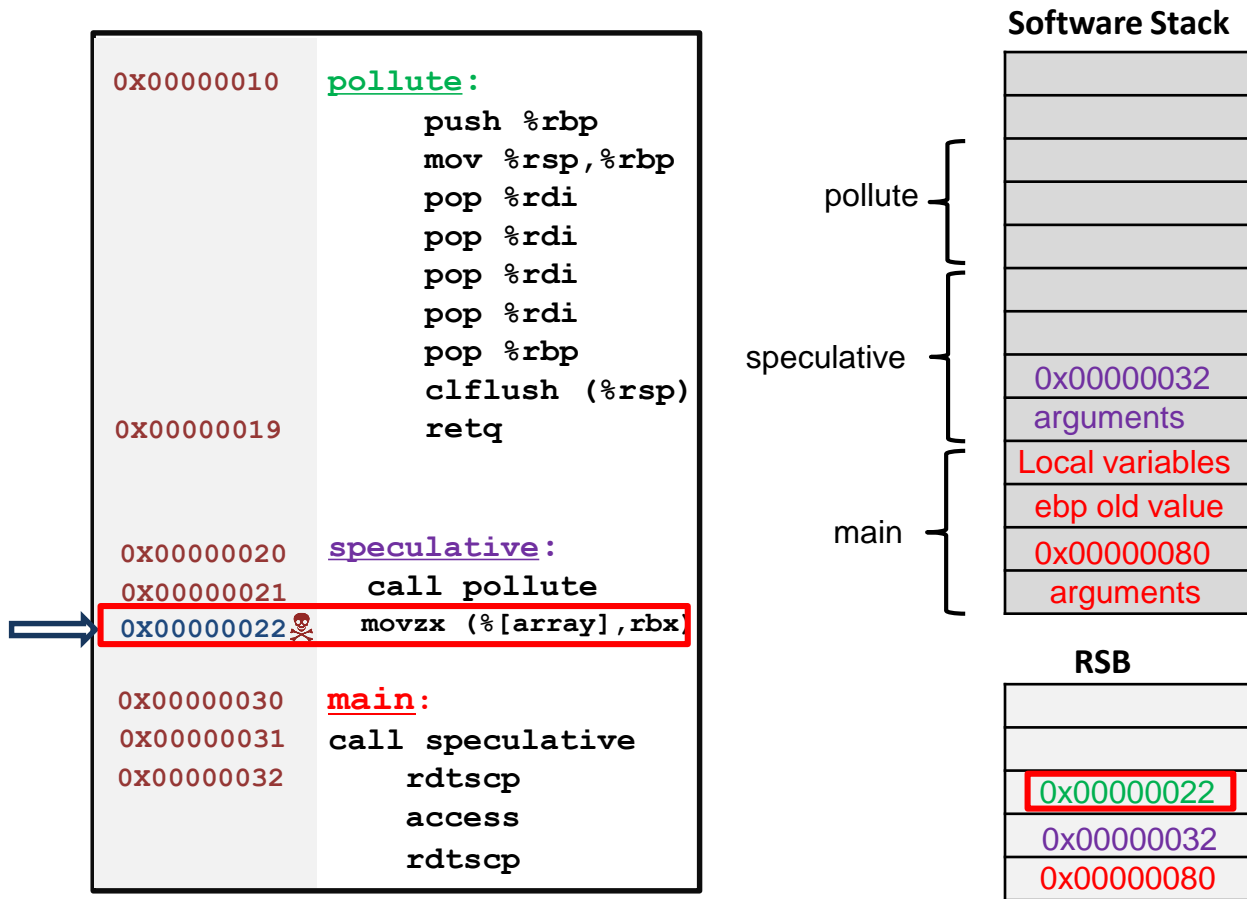
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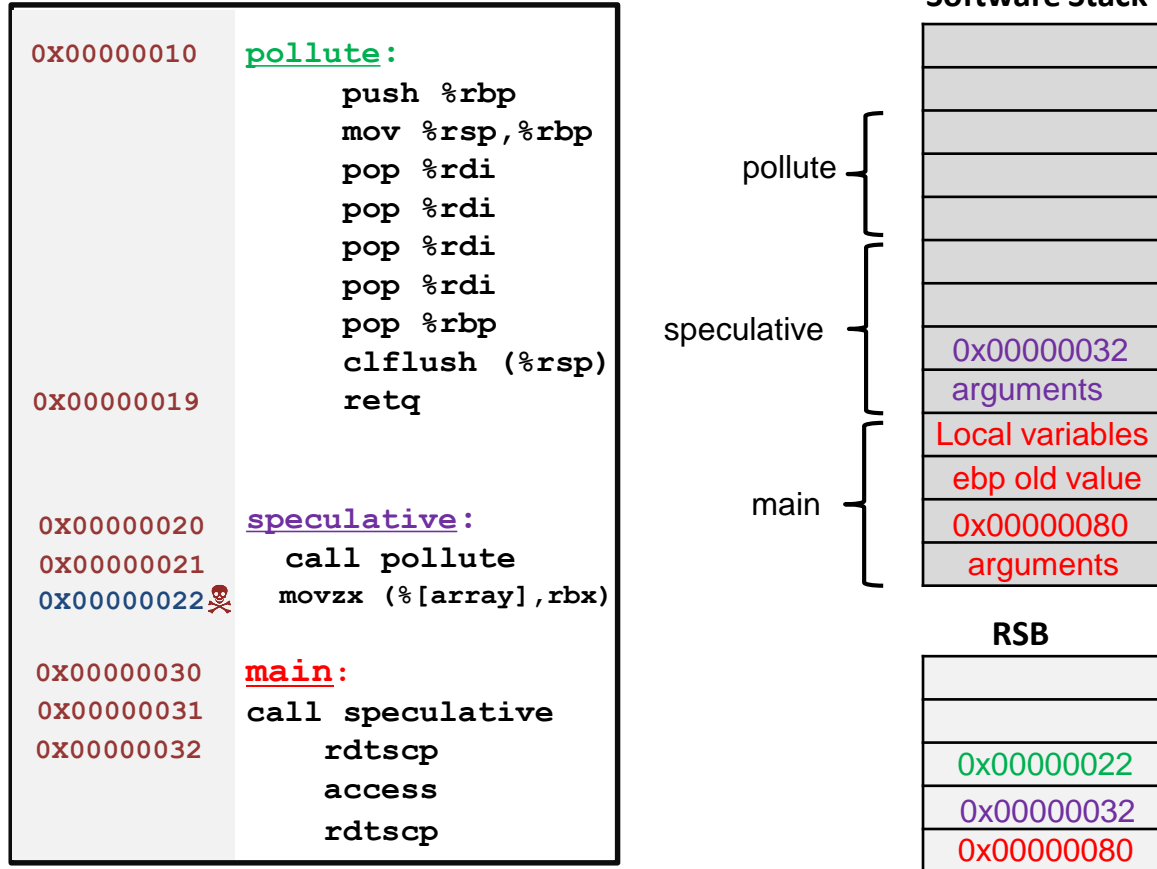
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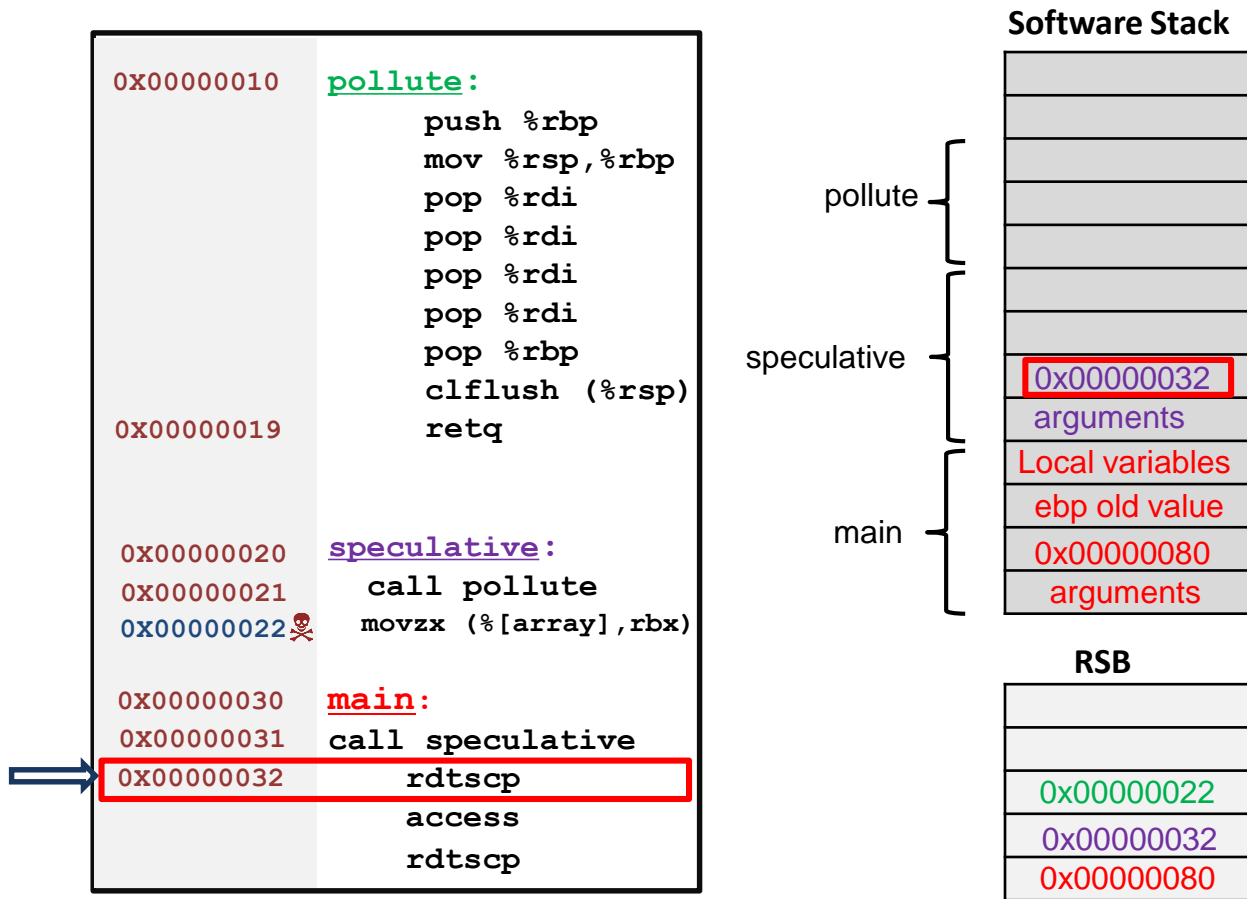
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# Defenses

- Microcode patches
  - Lfence
  - IBRS
  - IBPB
- Software patches
  - Retpoline
  - RSBstuffing





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- **Indirect Branch Predictor Barrier (IBPB)**
  - To prevent software running before the barrier to affect the indirect branch prediction of software running after the barrier

# Software Patch: RSB refilling

- RSB underfill (Skylake+)

```
void rsb_stuff(void) {  
    asm(".rept 16\n" "call 1f\n"  
        "pause ; lfence\n"  
        "1: \n"  
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# Software Patch: RSB refilling

- RSB underfill (Skylake+)
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  - Enables attacker to bypass defense
  - Fill the RSB with a sequence of benign address

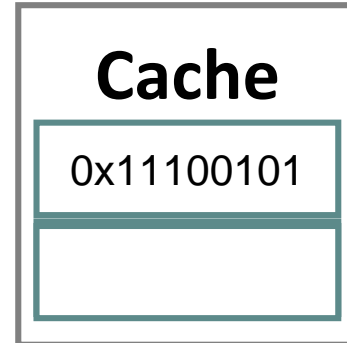
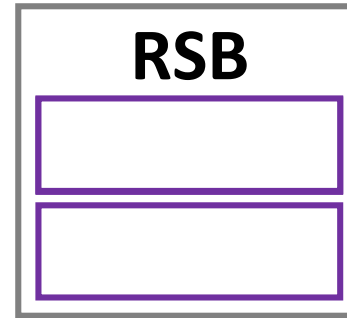
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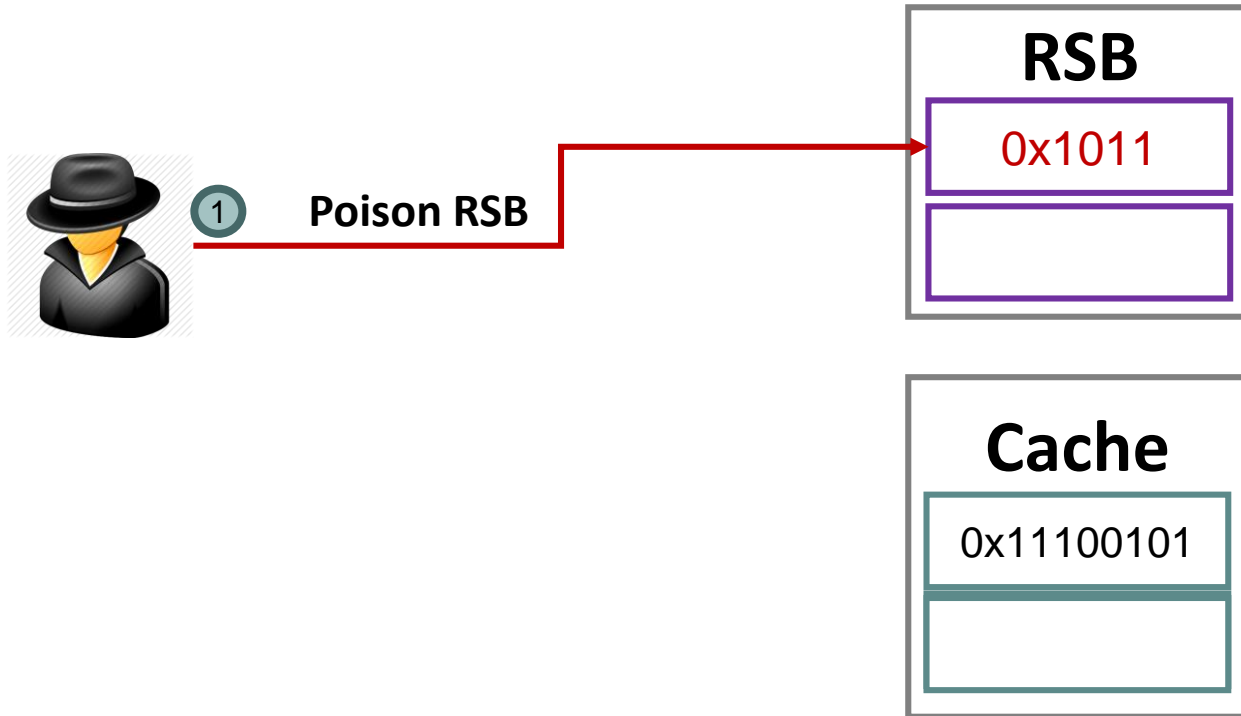
# Attack 2: Across different threads/process

- **Attack setup:**
  - The attacker and victim run on a same core (Share RSB)
  - Synchronize threads using futex operations to control their interleaving

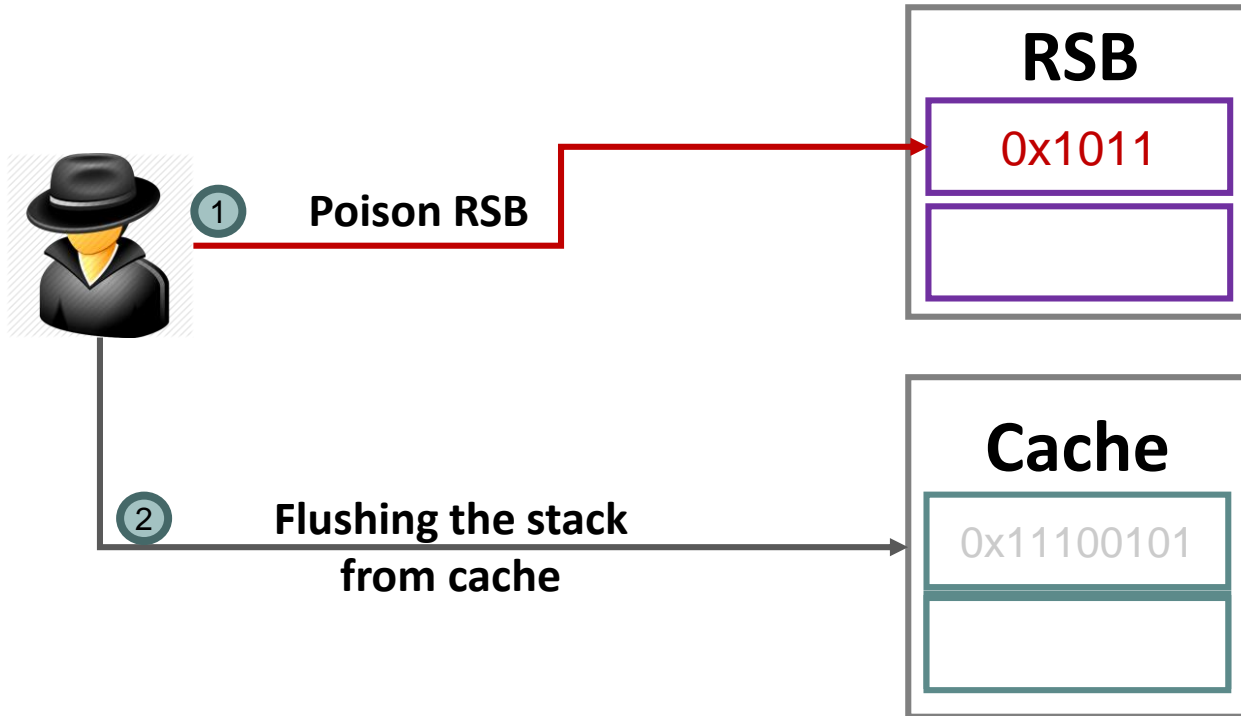
# Attack 2.a: Colluding threads (User)



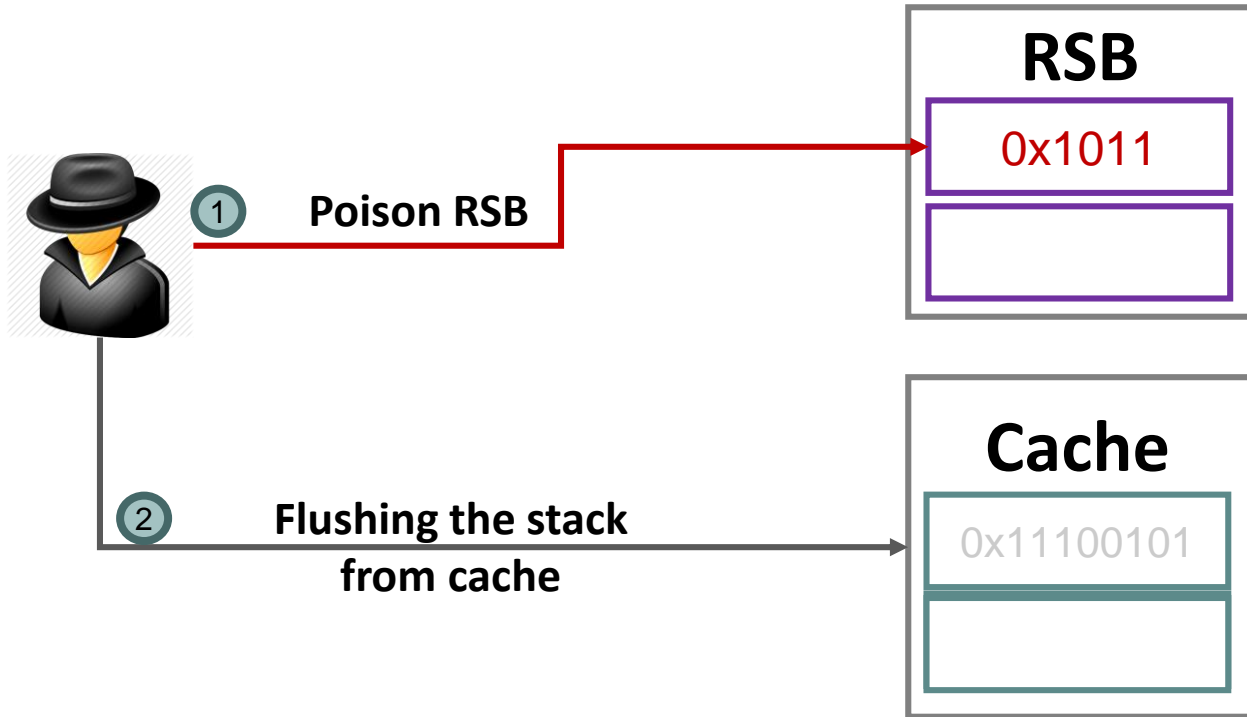
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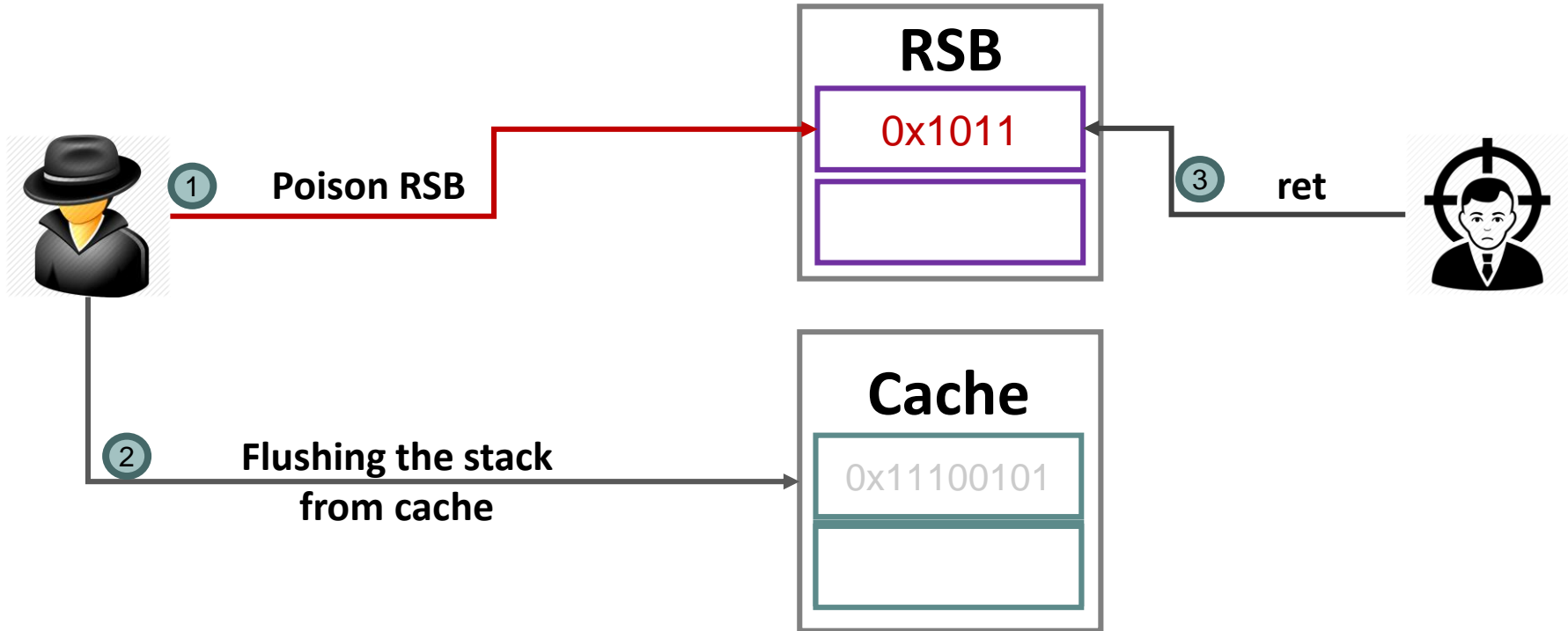
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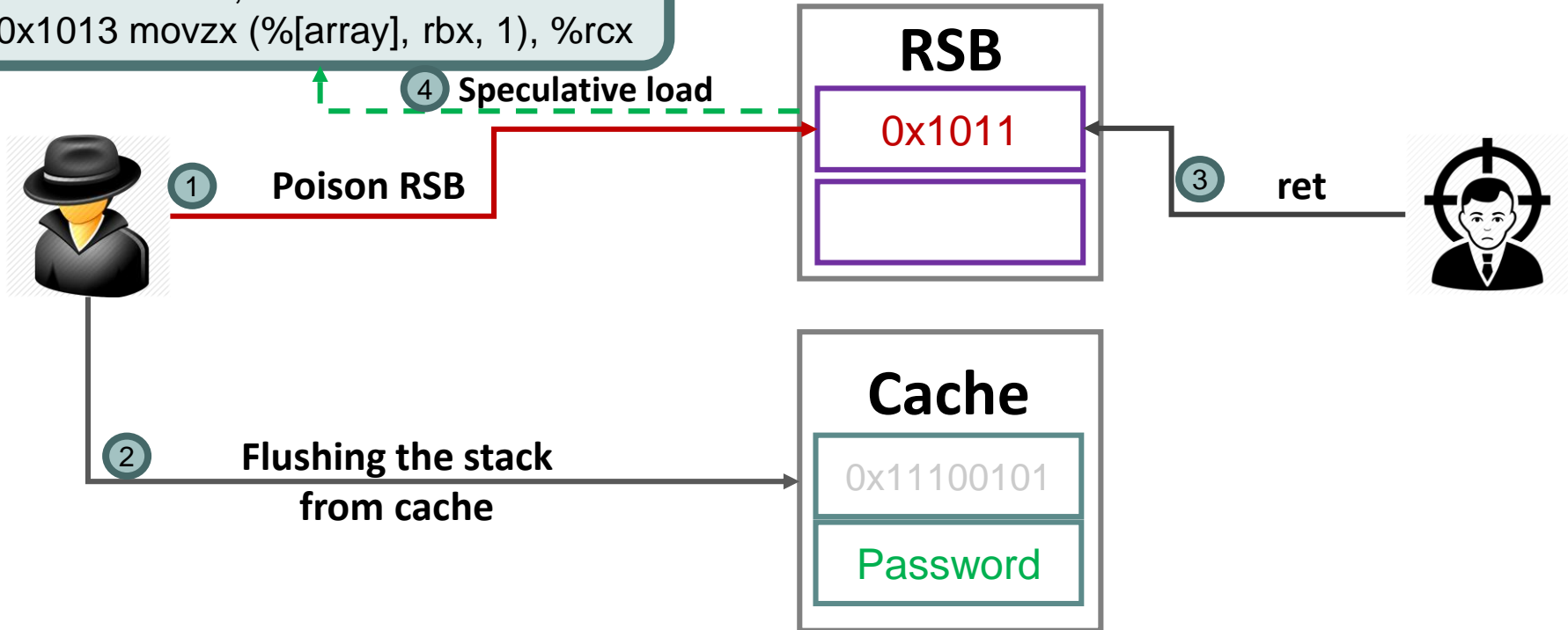


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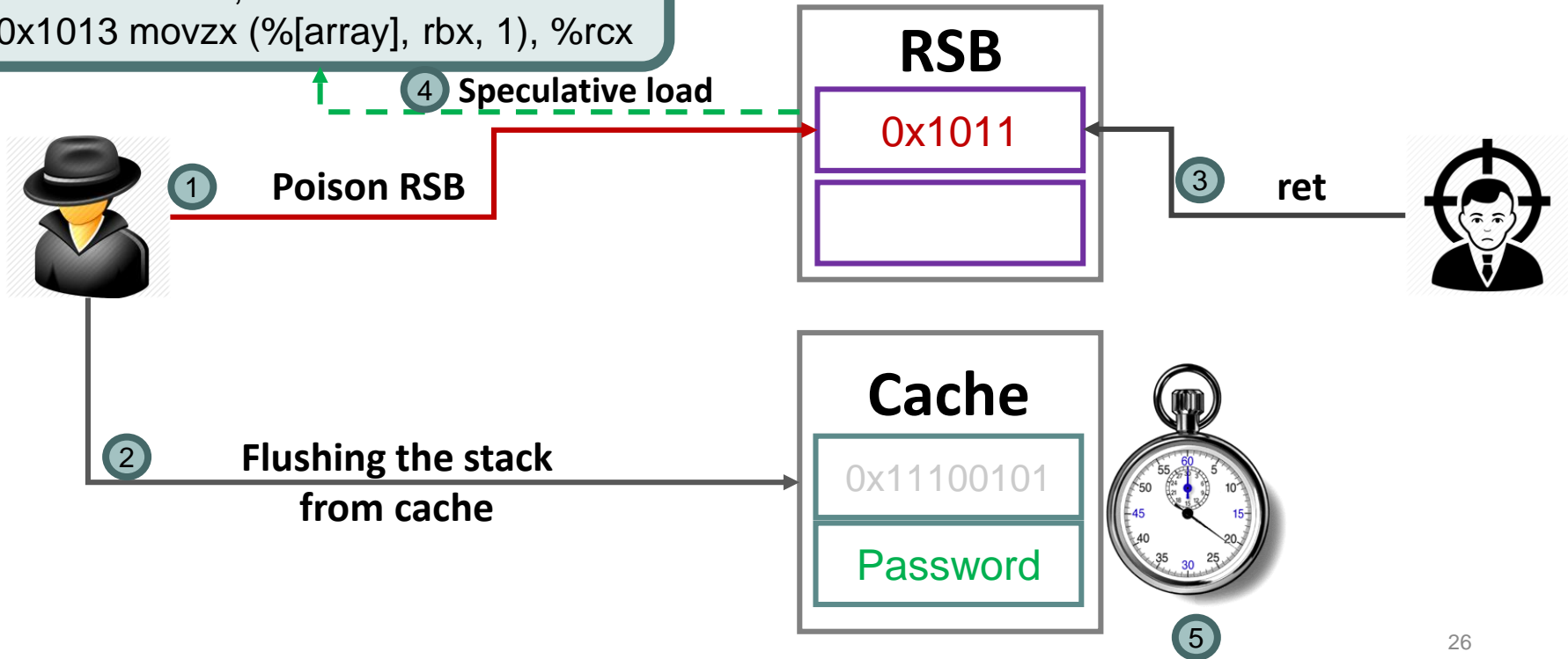
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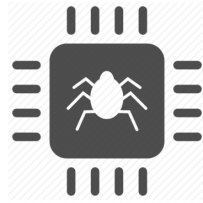
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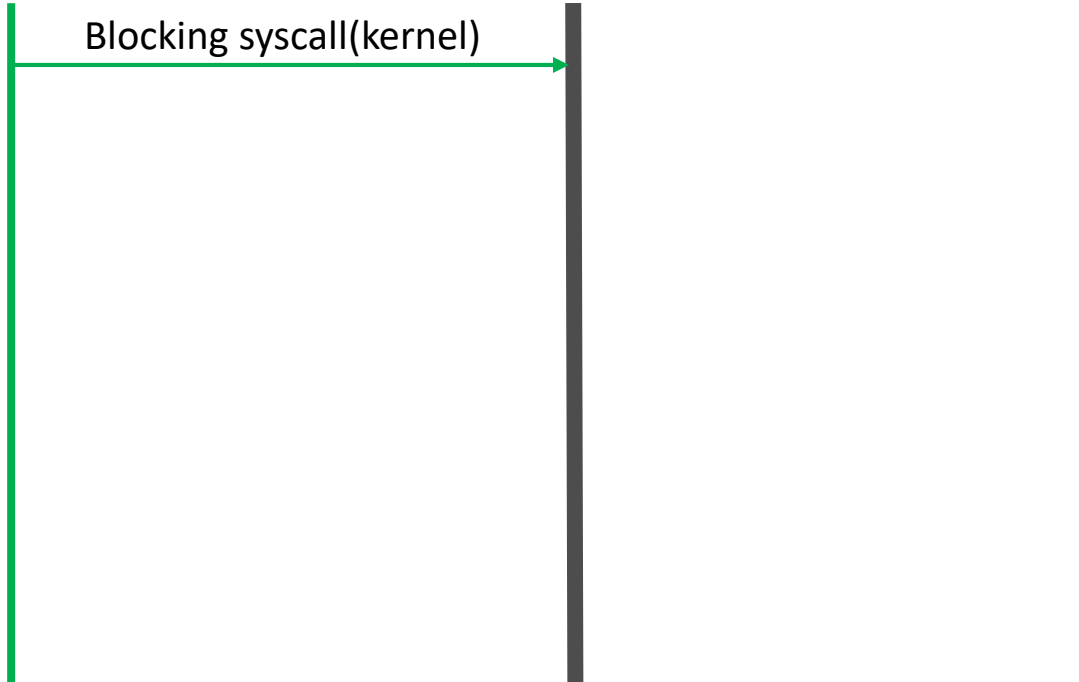
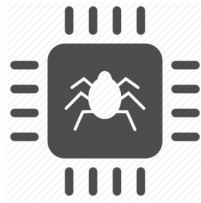




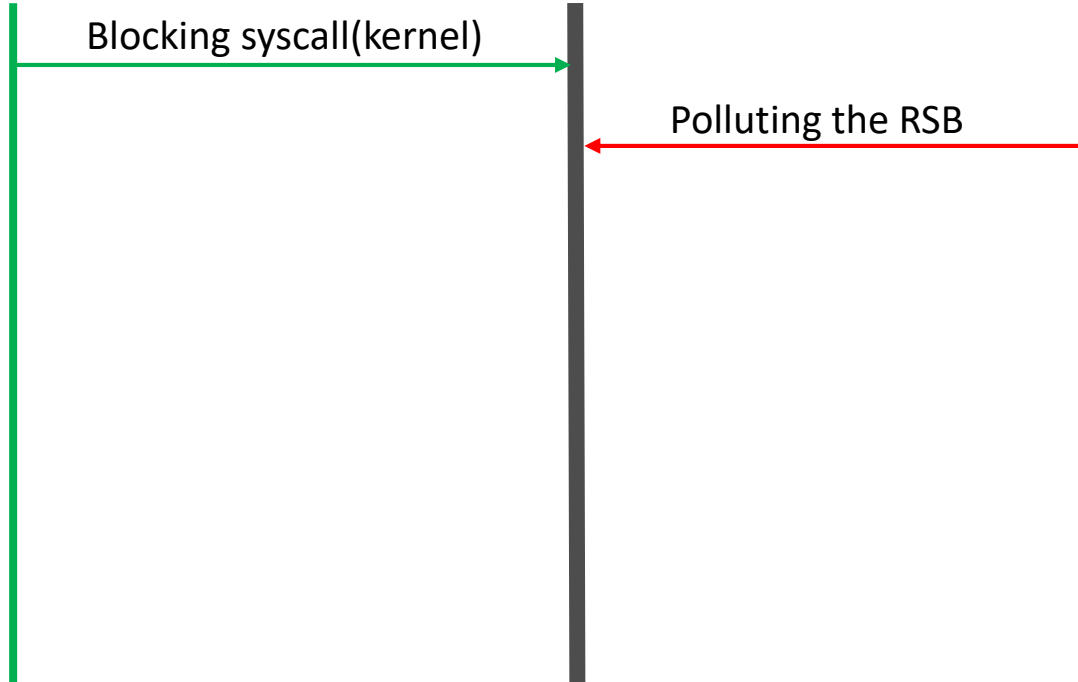
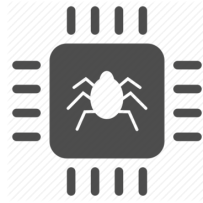
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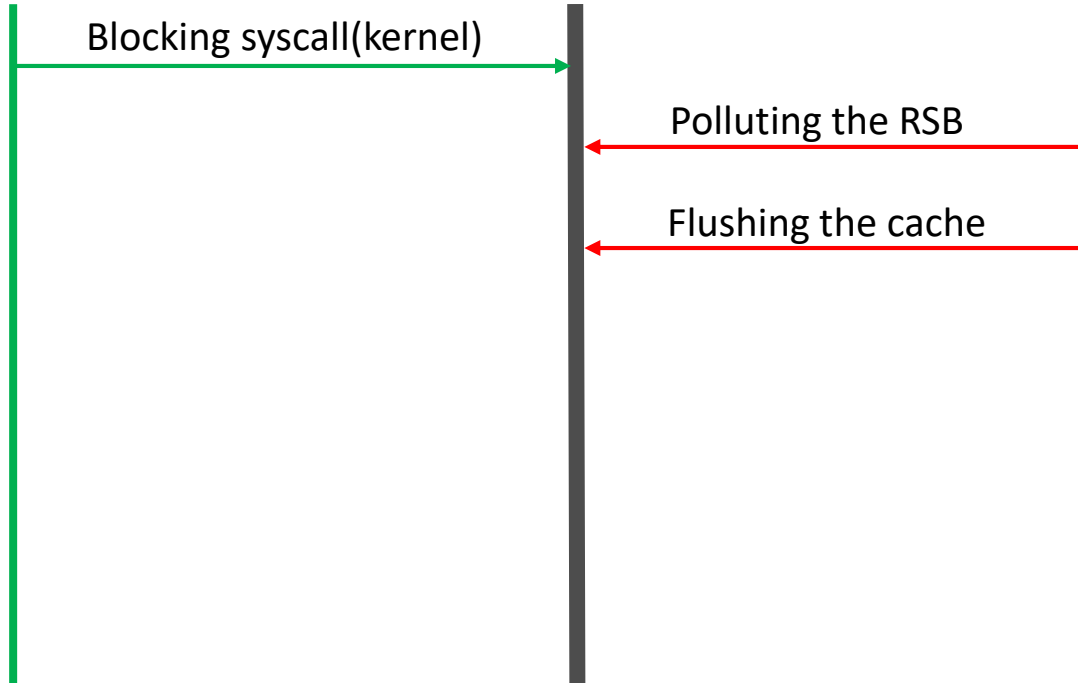
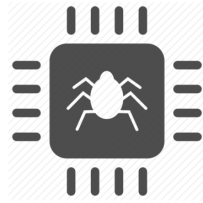
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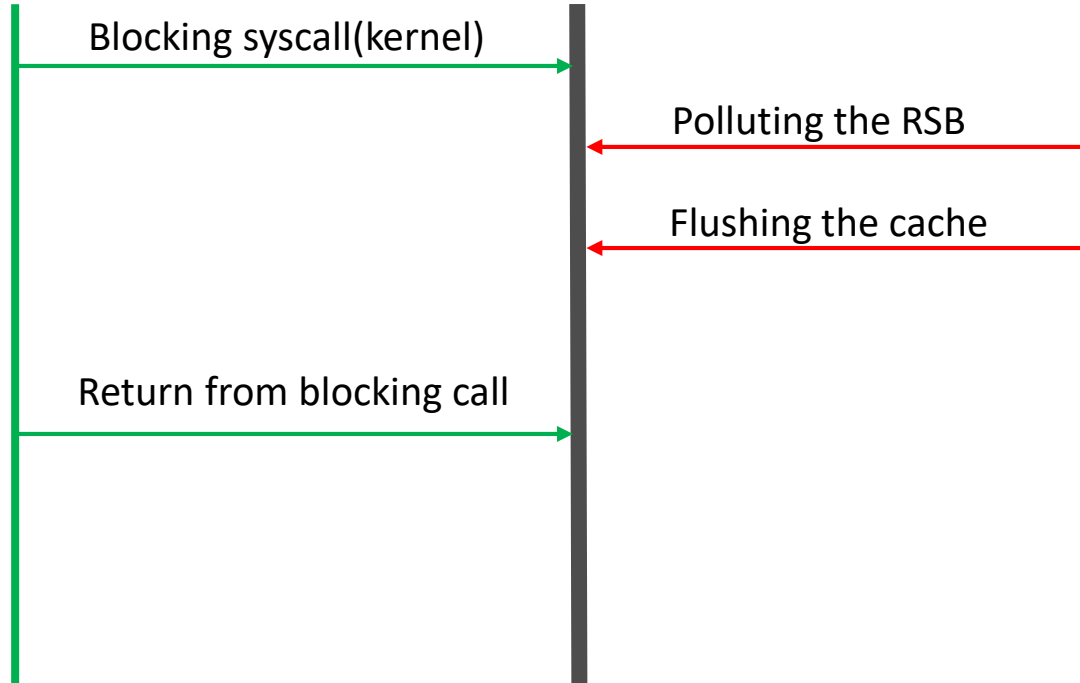
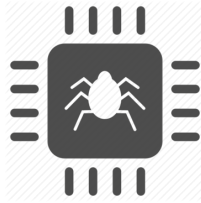
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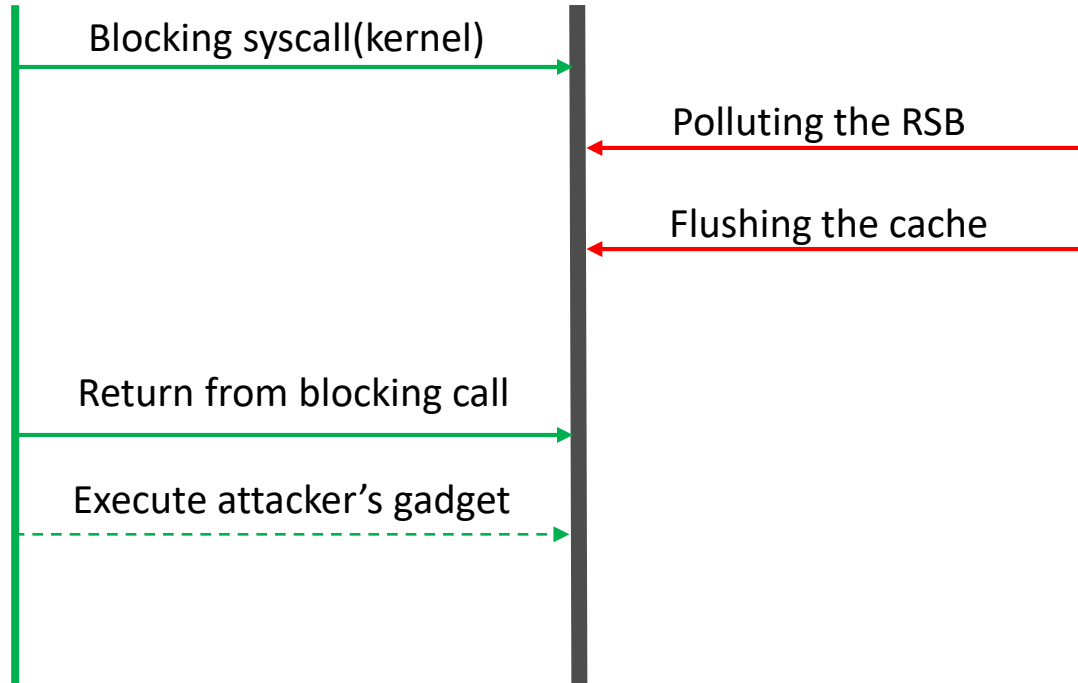
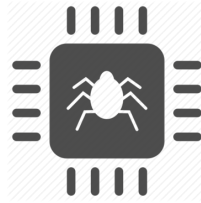
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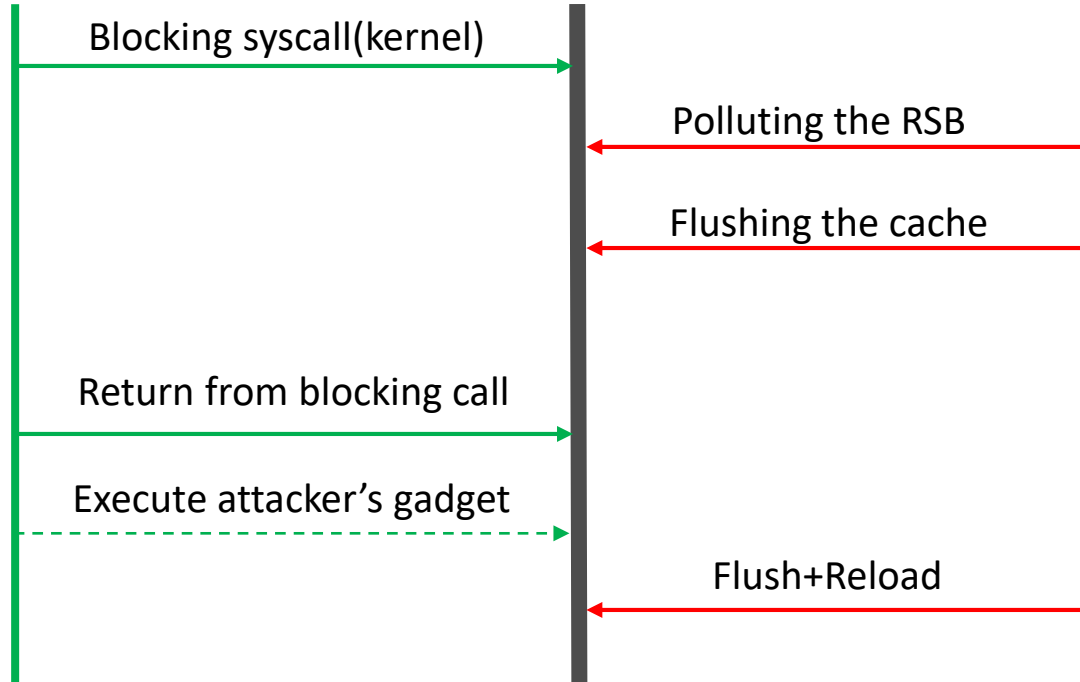
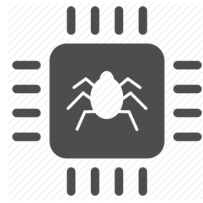
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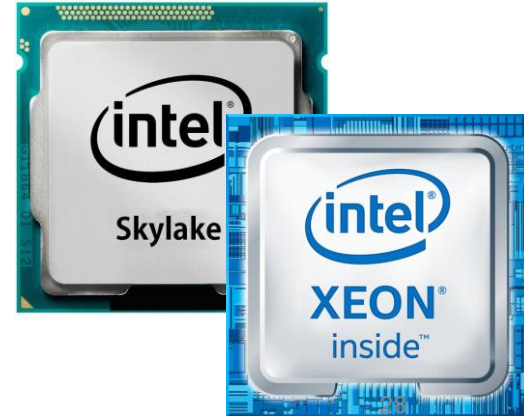
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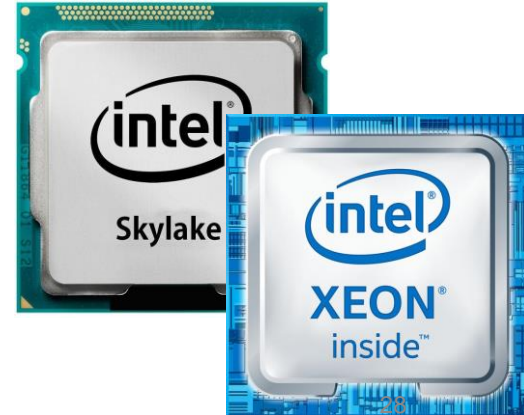
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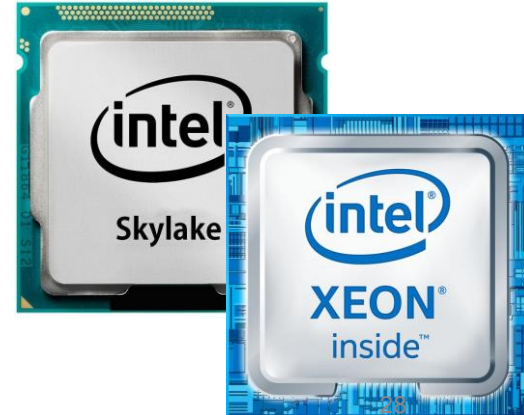
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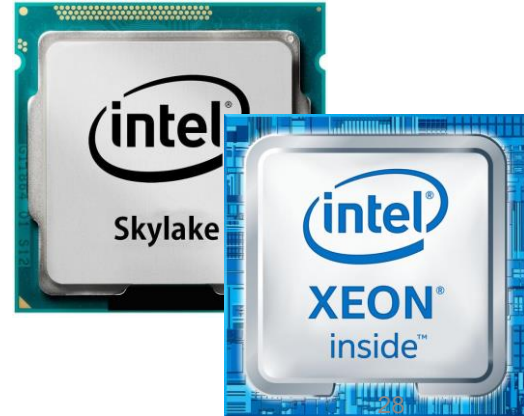
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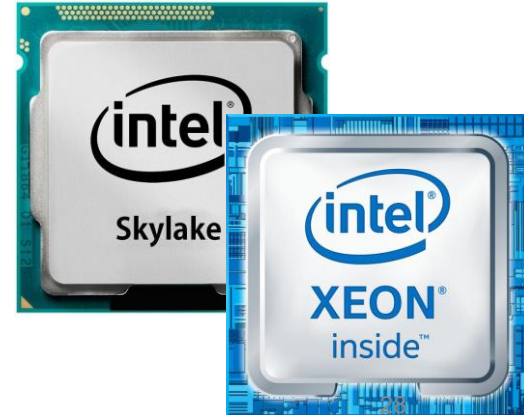
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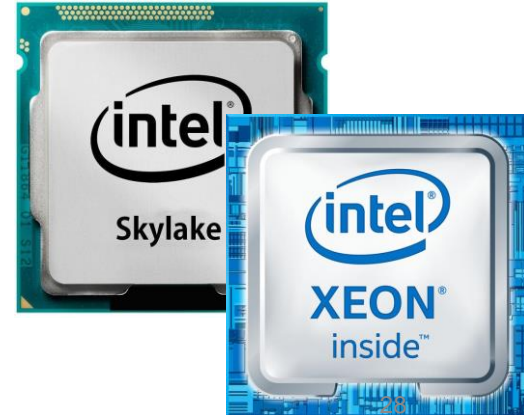
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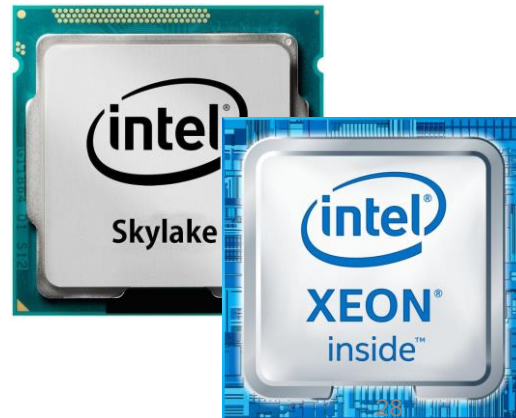
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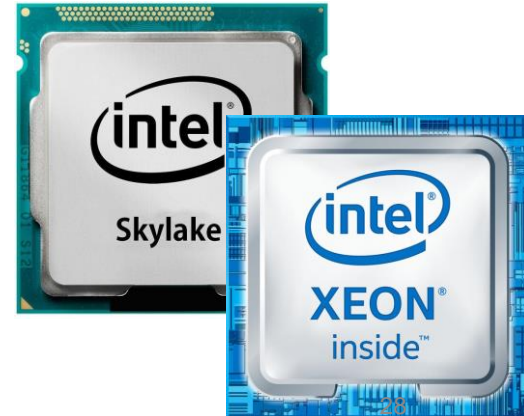
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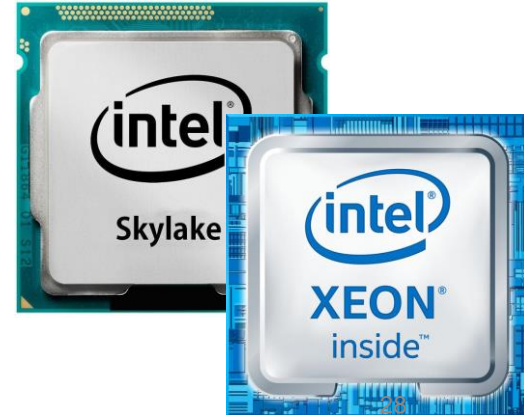
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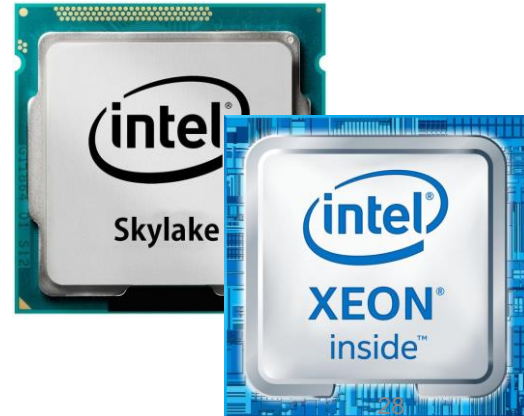
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- Does it issue in correct place?
- Does IBPB reset the RSB in the latest microcode version?

# Other Attack Scenarios

## Attack on SGX

- Reveal Data from SGX enclave
- Triggering an unmatched return
- IBPB prevent it based on the new contact with Intel engineer.

## Attack on other process

- Run on the same core
- Need to know the address of victim's stack
- Bypassing ASLR
- RSB refilling/IBPB may stop the attack

# Conclusion

- We introduced a new variant of Spectre attack which exploits Return Stack buffer
- Discussed different types of SpectreRSB against existing microcode and software patches

# Thank you!

## Questions?

