

Collide+Power: Leaking Inaccessible Data with Software-based Power Side Channels

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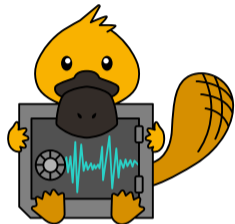
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CISPA

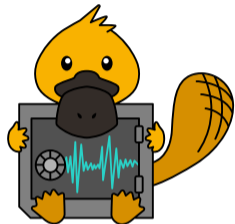
Stefan Mangard

TU-Graz



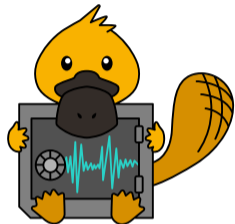


Software-based Power Side Channels



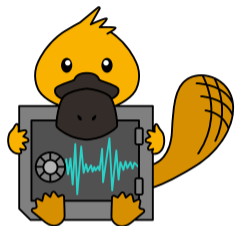
Software-based Power Side Channels

- **Specific** targets: AES



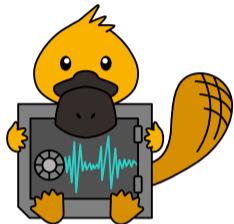
Software-based Power Side Channels

- **Specific** targets: AES
- Leak edge cases: RSA, SIKE, KASLR



Software-based Power Side Channels

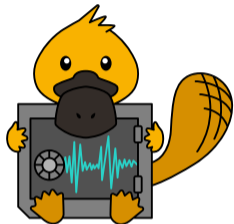
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Transient Execution Attacks

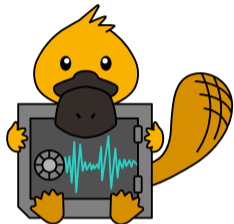


Software-based Power Side Channels

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Transient Execution Attacks

- **Generic** targets: CPU components

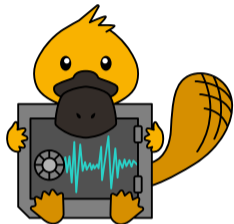


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- Leak arbitrary data: Cache content

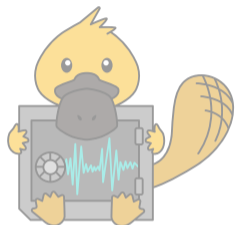


Software-based Power Side Channels

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- Leak edge cases: RSA, SIKE, KASLR
- **Limited** to a side channels

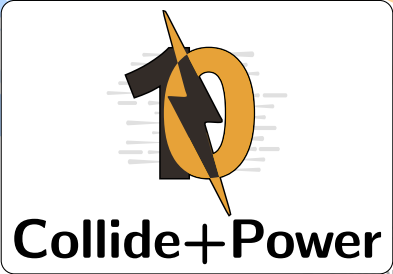
Transient Execution Attacks

- **Generic** targets: CPU components
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Software-based Power Side-Channel Attacks

- **Specific** targets: AES
- Leak edge cases: RSA, SIKE, KASLR
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Collide+Power

Execution Attacks

- **Generic** targets: CPU components
- Leak arbitrary data: Cache content
- **Agnostic** to side channels



High-Level Idea





Hamming Weight: $hw(x)$



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Number of set bits



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Number of set bits

$$hw(11_2) = 2$$



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Hamming Distance: $hd(x, y)$



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Hamming Distance: $hd(x, y)$

Number of different bits



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Number of set bits

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Hamming Distance: $hd(x, y)$

Number of different bits

$$hd(11_2, 01_2) = 1$$



- **Collide+Power** exploits leakage between:



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 - **Guess** \mathcal{G} : Attacker-controlled data
 - **Value** \mathcal{V} : Victim secret data
- 💡 Hamming distance: $\text{hd}(\mathcal{G}, \mathcal{V})$
- **How to exploit this limited information?**



$$\mathcal{P}(\mathcal{G}, \mathcal{V}) \approx \dots$$

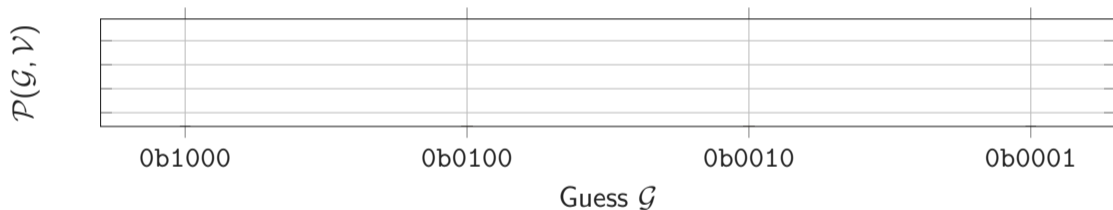
$$\mathcal{P}(\mathcal{G}, \mathcal{V}) \approx \text{hd}(\mathcal{G}, \mathcal{V})$$

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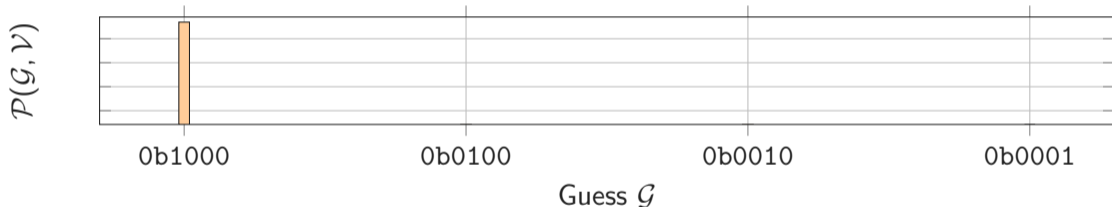
$$\underbrace{\mathcal{P}(\mathcal{G}, \mathcal{V})}_{\text{model}} \approx \text{hd}(\mathcal{G}, \mathcal{V})$$

$$\underbrace{\mathcal{P}(\mathcal{G}, \mathcal{V})}_{\text{model}} \approx \underbrace{\text{hd}(\mathcal{G}, \mathcal{V})}_{\text{signal}}$$

$$\mathcal{P}(\mathcal{G}, 0101_2) \approx \text{hd}(\mathcal{G}, 0101_2)$$

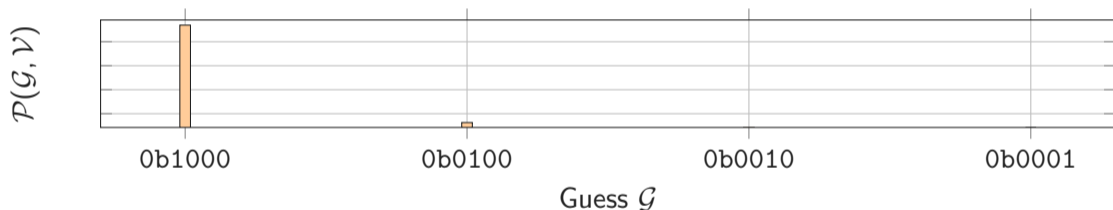


$$\mathcal{P}(1000_2, 0101_2) \approx \text{hd}(\mathbf{1}000_2, \mathbf{0}101_2) = 3$$

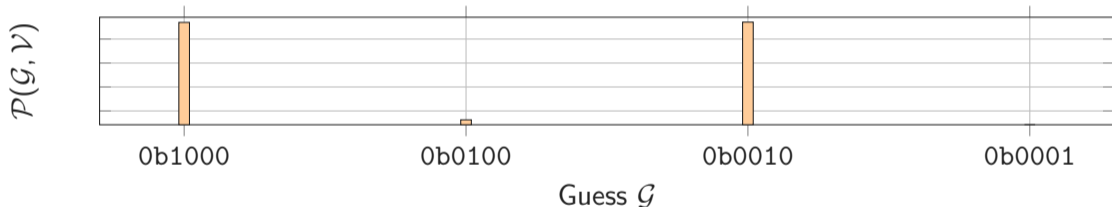




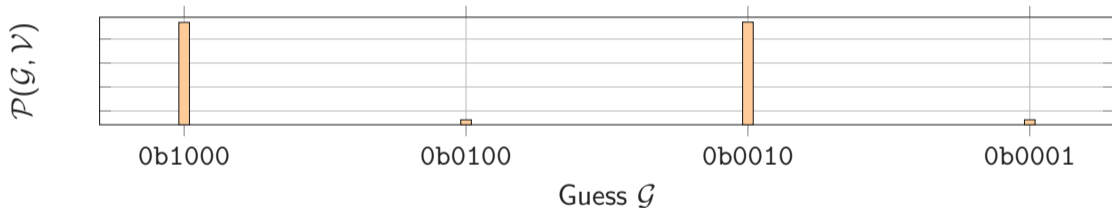
$$\mathcal{P}(0100_2, 0101_2) \approx \text{hd}(0\mathbf{1}00_2, 0\mathbf{1}01_2) = 1$$

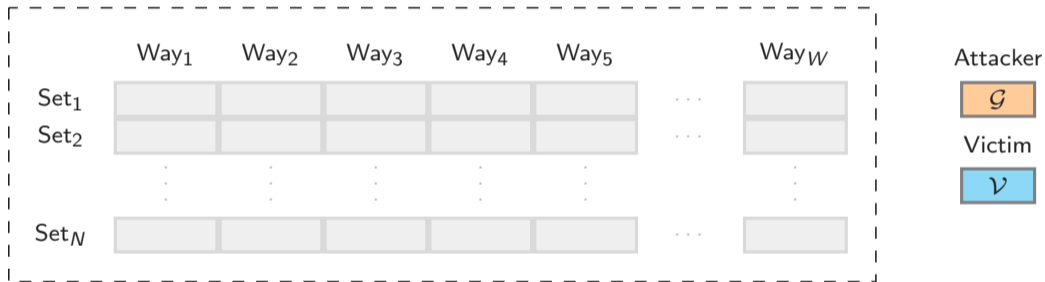


$$\mathcal{P}(0010_2, 0101_2) \approx \text{hd}(00\mathbf{1}0_2, 01\mathbf{0}1_2) = 3$$

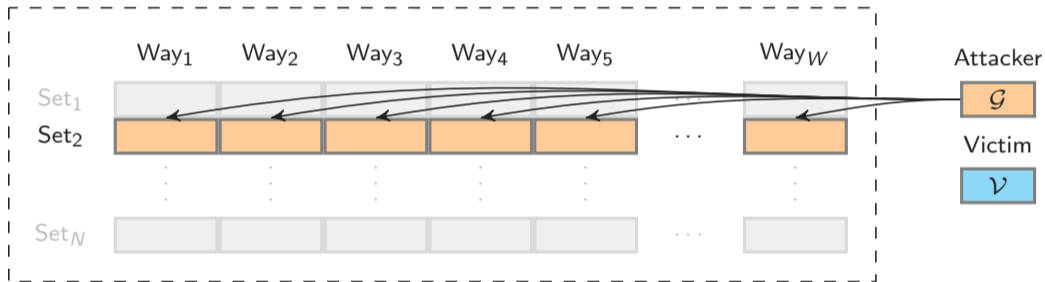


$$\mathcal{P}(0001_2, 0101_2) \approx \text{hd}(000\mathbf{1}_2, 010\mathbf{1}_2) = 1$$

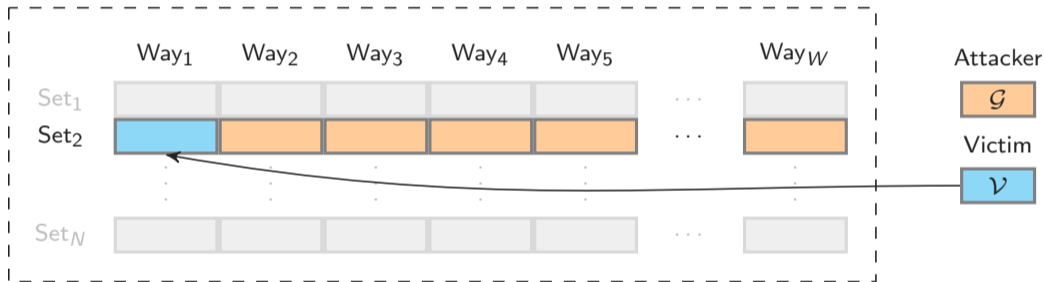


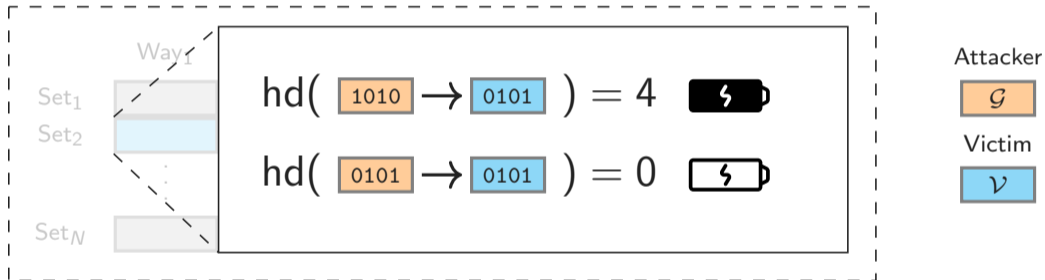


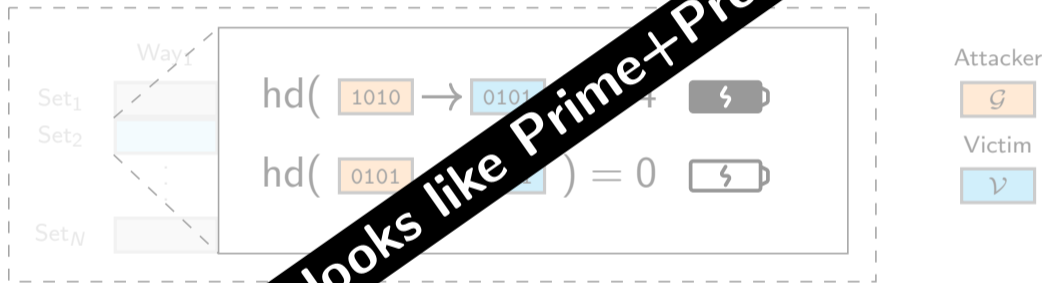
Collide+Power - Memory Subsystem



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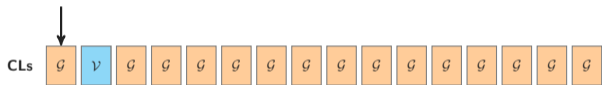


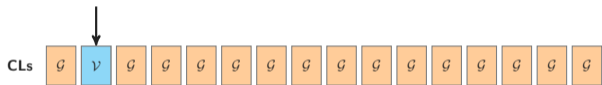


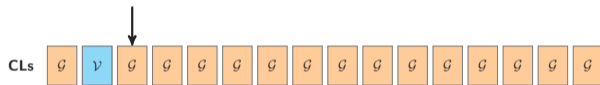


Leakage Analysis

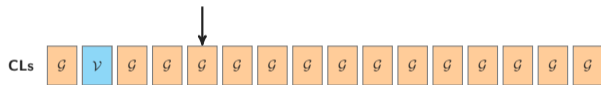




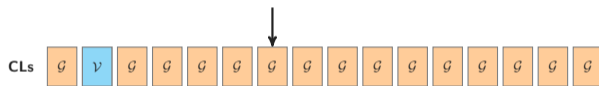


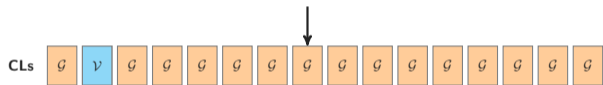


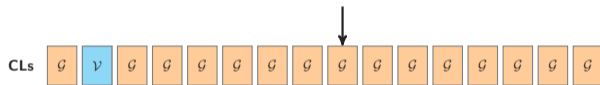


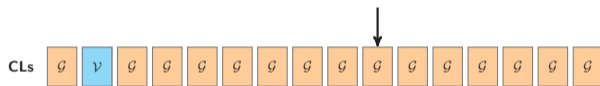


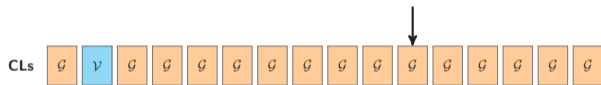




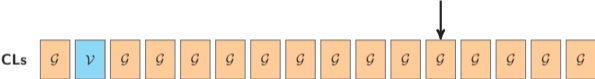






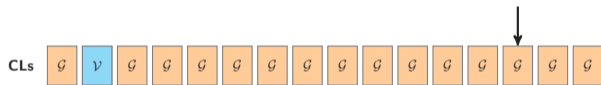


Leakage Analysis - Experiment Setup

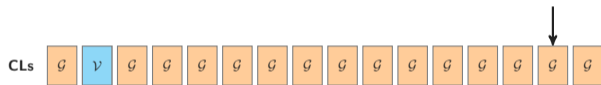


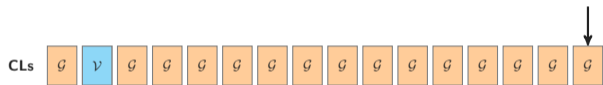
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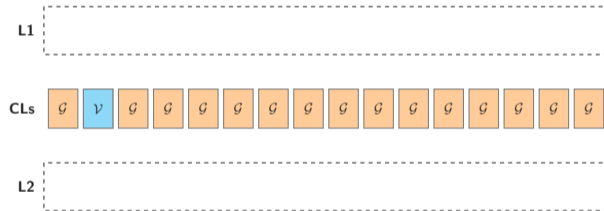
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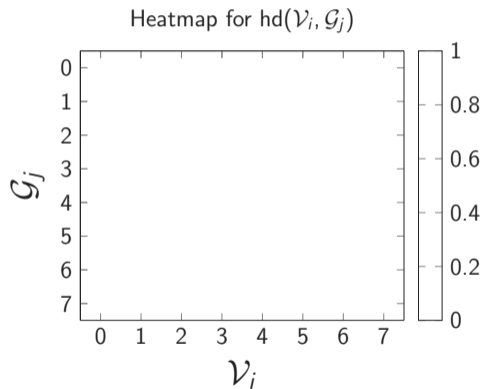
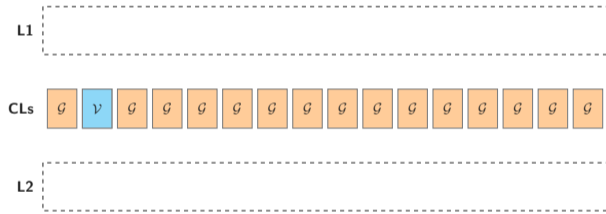




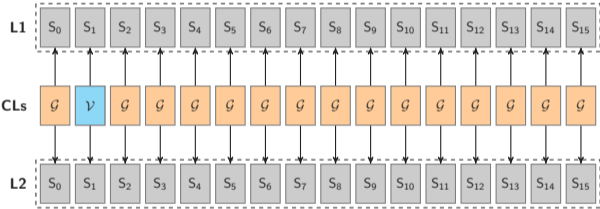


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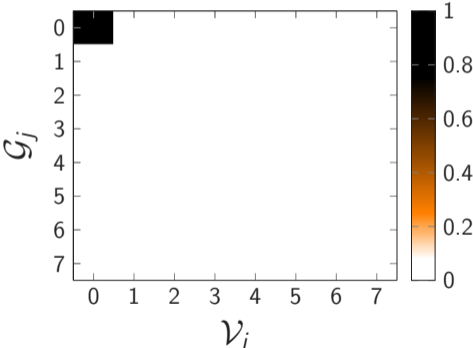




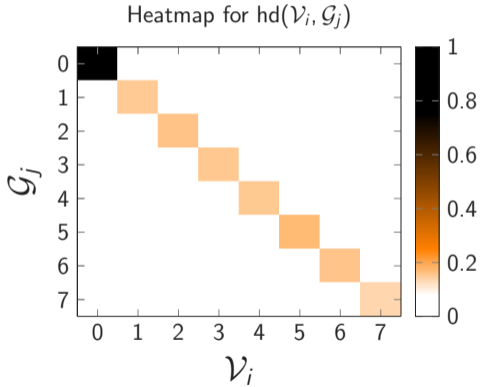
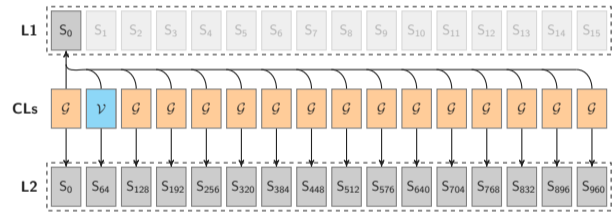
Leakage Analysis - No Eviction



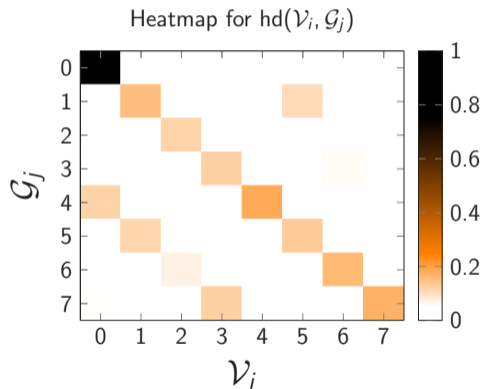
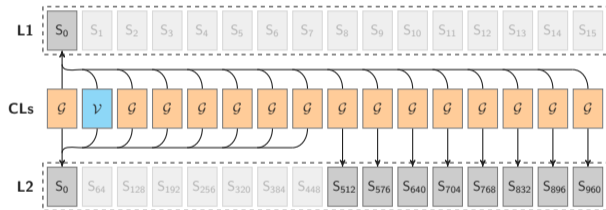
Heatmap for $hd(\mathcal{V}_i, \mathcal{G}_j)$



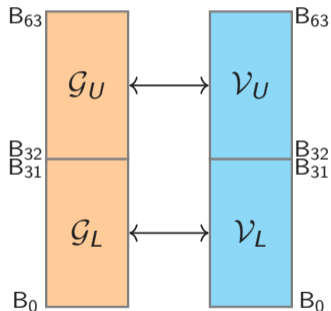
Leakage Analysis - L1 Eviction



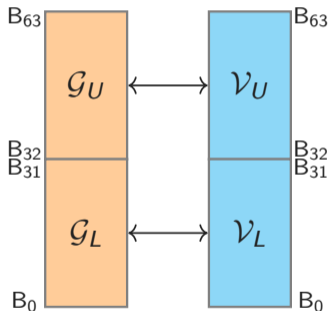
Leakage Analysis - L1+L2 Eviction



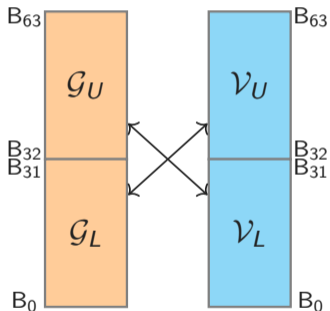
Aligned Leakage



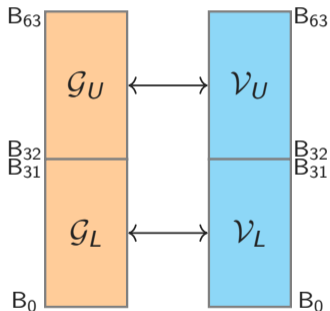
Aligned Leakage



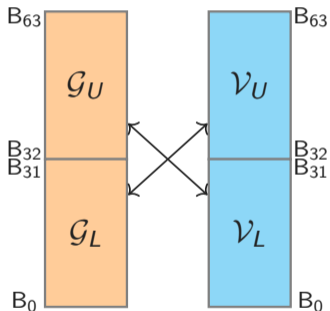
Cross Leakage



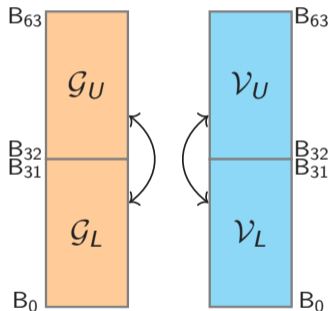
Aligned Leakage



Cross Leakage



Self Leakage

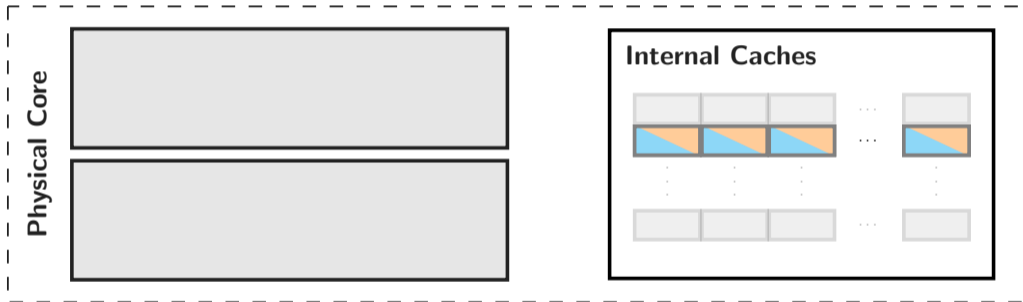


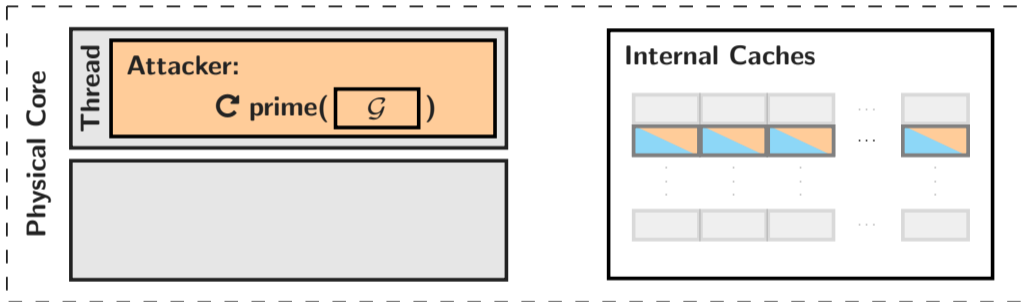
Leakage Analysis: Results

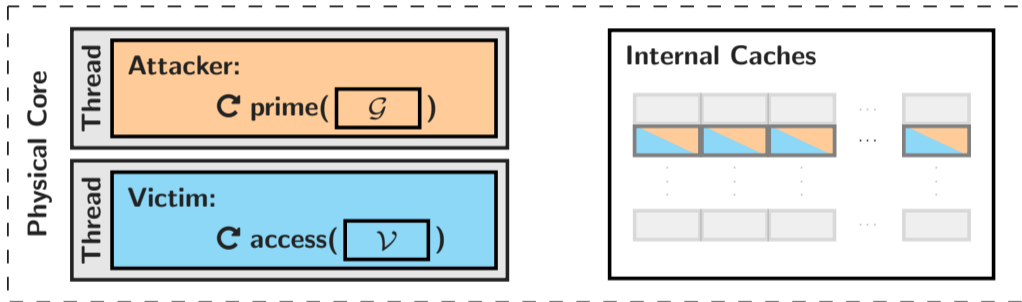
Inst.	Evict.	Effectiveness		Aligned Leakage		Cross Leakage		Self Leakage		Weights			
		$\hat{\rho}$ ·1	SNR_A ·10 ⁻³	$\text{hd}(v_L, g_L)$ a_0 in μW	$\text{hd}(v_U, g_U)$ a_1 in μW	$\text{hd}(v_L, g_U)$ c_0 in μW	$\text{hd}(v_U, g_L)$ c_1 in μW	$\text{hd}(v_L, v_U)$ s_0 in μW	$\text{hd}(g_L, g_U)$ s_1 in μW	$\text{hw}(v_L)$ w_0 in μW	$\text{hw}(v_U)$ w_1 in μW	$\text{hw}(g_L)$ w_2 in μW	$\text{hw}(g_U)$ w_3 in μW
Load	None	0.311	72.004	544.5	4.2	1.1	0.5	0.0	0.0	0.0	0.0	362.6	0.0
	L1	0.907	7.873	598.3	278.8	0.0	0.0	0.0	0.0	0.0	0.0	6124.4	2696.9
	L1+L2	0.822	5.632	339.3	141.7	106.6	43.0	0.0	0.0	0.0	0.0	3750.7	1435.0
Prefetch	None	0.003	0.000	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	1.7	2.8
	L1	0.370	11.365	136.0	63.3	40.9	43.0	0.1	0.0	0.0	0.0	454.1	455.5
	L1+L2	0.300	5.290	133.7	169.0	40.9	43.0	0.0	0.0	0.0	0.0	334.0	332.5
Store	None	0.003	0.000	0.0	0.0	0.0	3.1	0.0	0.0	0.0	0.0	7.0	0.0
	L1	0.241	3.876	63.3	74.5	4.9	9.6	0.0	0.0	0.0	0.0	204.6	303.2
	L1+L2	0.450	6.457	133.7	169.0	84.7	86.2	0.0	0.0	0.0	0.0	347.1	1130.5

Do not start reading this!

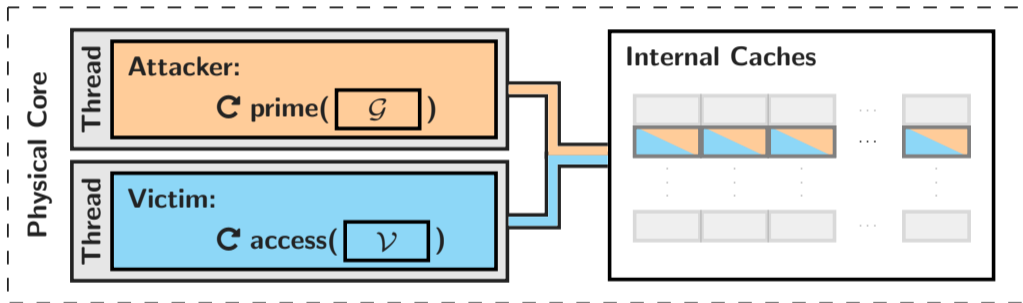
Generic Attacks





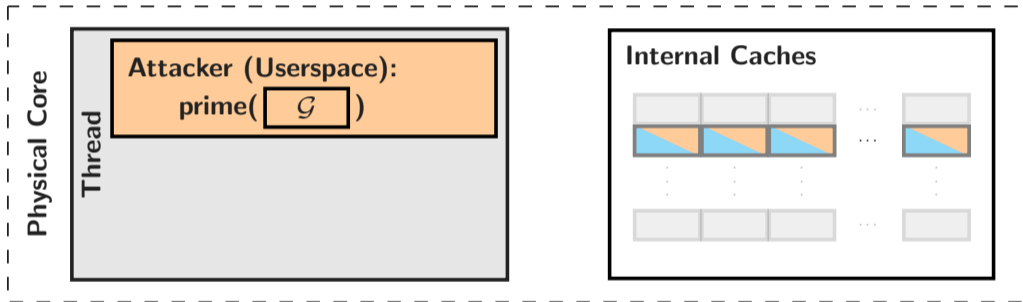


MDS-style Attack

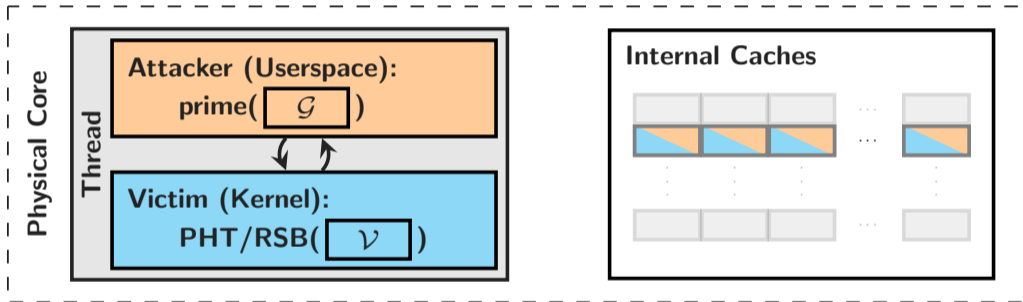




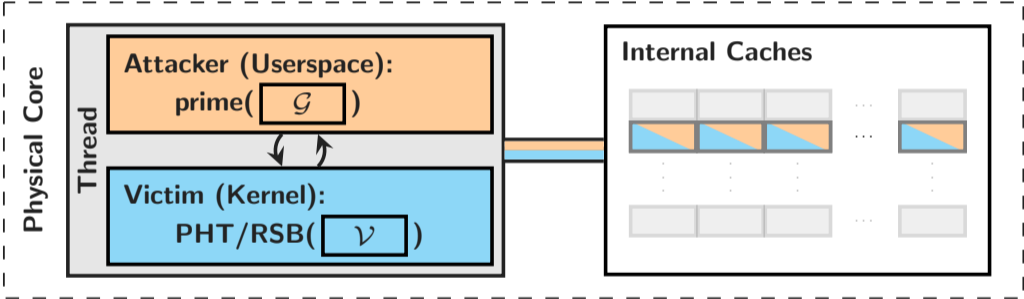
Meltdown-style Attack



Meltdown-style Attack



Meltdown-style Attack



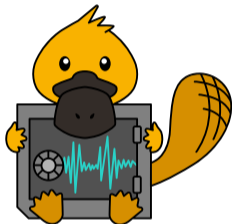
This must be slow?

NO!

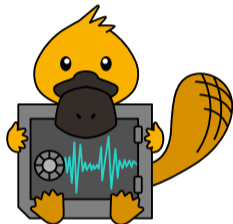
It is **EXTREMELY** slow!¹

¹With the current state-of-the-art.

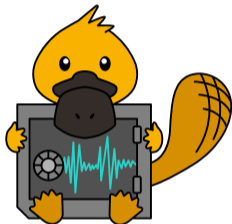




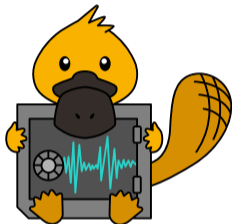
- Direct power measurements



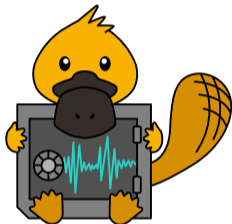
- Direct power measurements
- Unprivileged Interface



- Direct power measurements
- ~~Unprivileged Interface~~



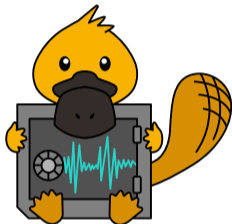
- Direct power measurements
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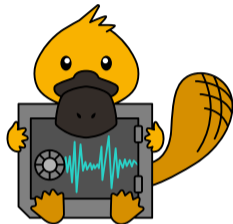
- Indirect power measurements



- Direct power measurements
- ~~Unprivileged Interface~~

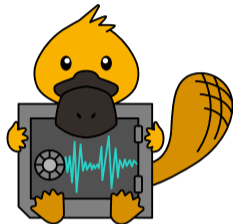


- Indirect power measurements
- Higher consumption → more throttling

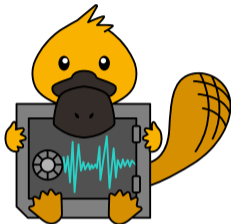


- **MDS-style:**

4.82 bit/h



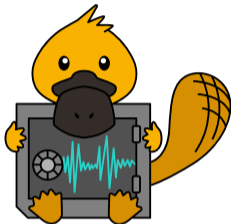
- **MDS-style:**
4.82 bit/h
- **Meltdown-style (RSB):**
0.84 bit/h



- **MDS-style:**
4.82 bit/h
- **Meltdown-style (RSB):**
0.84 bit/h



- **MDS-style:**
0.065 to 0.68 bit/h



- **MDS-style:**
4.82 bit/h
- **Meltdown-style (RSB):**
0.84 bit/h



- **MDS-style:**
0.065 to 0.68 bit/h
- **Meltdown-style estimate (PHT):**
99.95 days/bit to 2.86 years/bit

🌐 Collide+Power: <https://collidepower.com>





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- For **more** details:
 - Prefetcher effects
 - Differential measurement
 - Even more evaluation ...



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Read the Paper